ANALOG DEVICES

ADSP-2100 Family DSP Microcomputers

ADSP-21xx

SUMMARY

16-Bit Fixed-Point DSP Microprocessors with On-Chip Memory
Enhanced Harvard Architecture for Three-Bus Performance: Instruction Bus & Dual Data Buses
Independent Computation Units: ALU, Multiplier/ Accumulator, and Shifter
Single-Cycle Instruction Execution & Multifunction Instructions
On-Chip Program Memory RAM or ROM & Data Memory RAM
Integrated I/O Peripherals: Serial Ports, Timer, Host Interface Port (ADSP-2111 Only)

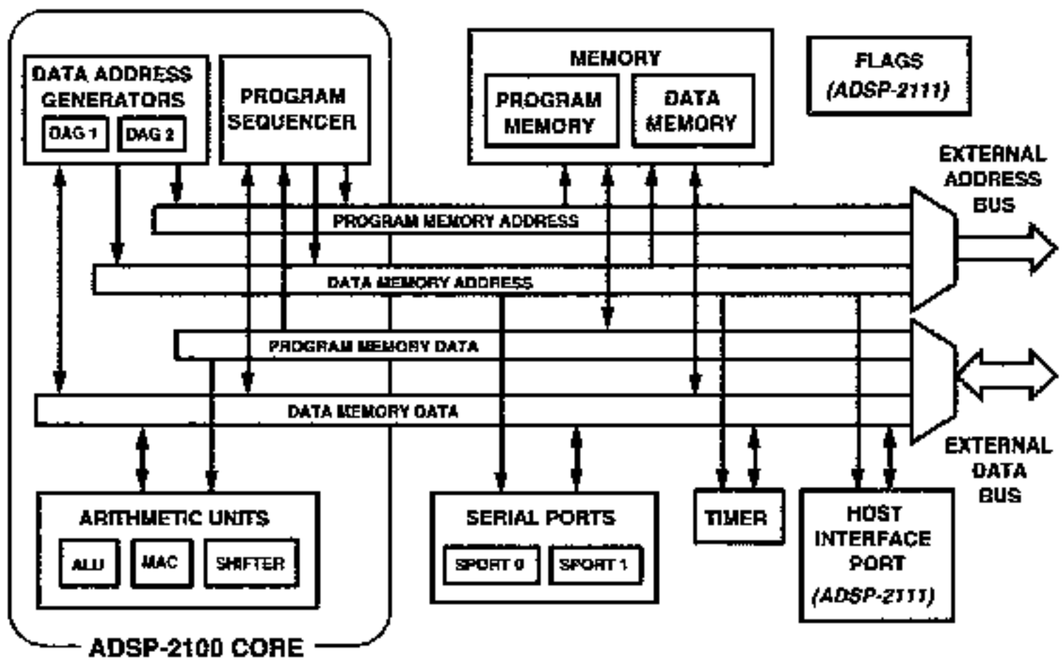
FEATURES

20 MIPS, 50 ns Maximum Instruction Rate
Separate On-Chip Buses for Program and Data Memory
Program Memory Stores Both Instructions and Data (Three-Bus Performance)
Dual Data Address Generators with Modulo and Bit-Reverse Addressing
Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory (e.g., EPROM)
Double-Buffered Serial Ports with Companding Hardware, Automatic Data Buffering, and Multichannel Operation
ADSP-2111 Host Interface Port Provides Easy Interface to 68000, 80C51, ADSP-21xx, Etc.
Automatic Booting of ADSP-2111 Program Memory Through Host Interface Port
Three Edge- or Level-Sensitive Interrupts
Low Power IDLE Instruction
PGA, PLCC, PQFP, and TQFP Packages
MIL-STD-883B Versions Available

GENERAL DESCRIPTION

The ADSP-2100 Family processors are single-chip microcomputers optimized for digital signal processing (DSP) and other high speed numeric processing applications. The ADSP-21xx processors are all built upon a common core, the ADSP-2100. Each processor combines the core DSP architecture—computation units, data address generators, and program sequencer—with differentiating features such as on-chip program and data memory RAM, a programmable timer, one or two serial ports, and, on the ADSP-2111, a host interface port.

FUNCTIONAL BLOCK DIAGRAM



This data sheet describes the following ADSP-2100 Family processors:

ADSP-2101	
ADSP-2103	*3.3 V Version of ADSP-2101*
ADSP-2105	*Low Cost DSP*
ADSP-2111	*DSP with Host Interface Port*
ADSP-2115	
ADSP-2161/62/63/64	*Custom ROM-programmed DSPs*

The following ADSP-2100 Family processors are *not* included in this data sheet:

ADSP-2100A	*DSP Microprocessor*
ADSP-2165/66	*ROM-programmed ADSP-216x processors with powerdown and larger on-chip memories (12K Program Memory ROM, 1K Program Memory RAM, 4K Data Memory RAM)*
ADSP-21msp5x	*Mixed-Signal DSP Processors with integrated on-chip A/D and D/A plus powerdown*
ADSP-2171	*Speed and feature enhanced ADSP-2100 Family processor with host interface port, powerdown, and instruction set extensions for bit manipulation, multiplication, biased rounding, and global interrupt masking*
ADSP-2181	*Newest ADSP-21xx processor with ADSP-2171 features plus 80K bytes of on-chip RAM configured as 16K words of program memory and 16K words of data memory.*

Refer to the individual data sheet of each of these processors for further information.