HOLT INTEGRATED CIRCUITS

HI-8590

September 1999

ARINC 429 LINE DRIVER AND LINE RECEIVER

DESCRIPTION

The HI-8590 is a CMOS integrated circuit with independent ARINC 429 line driver and line receiver in a single 16 pin package. Both ARINC 429 functions are implemented in analog/digital CMOS.

The line driver function in the HI-8590 connects directly to the ARINC bus and translates CMOS/TTL input levels to ARINC 429 specified amplitudes using built-in zeners. The slope of the differential output signal is controlled by a single logic input without the use of any external capacitors. A internal 37.5 ohm resistor is provided in series with each line driver output. The line driver function is the same as Holt's 8 pin stand-alone HI-8585 line driver.

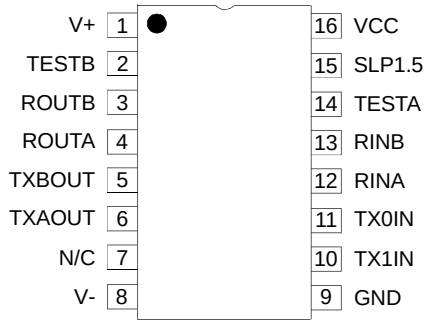
The line receiver interfaces directly to the ARINC 429 bus and translates incoming ARINC levels to levels compatible with CMOS logic. Internal comparator levels are set just below the standard 6.5 volt minimum data threshold and just above the standard 2.5 volt maximum null threshold

The TESTA and TESTB inputs of the line receiver allow bypassing the analog input circuitry for testing purposes. Also, if both test inputs are taken high, the analog circuitry powers down and the receiver's digital outputs are tri-stated allowing wire-or possibilities. The line driver function is the same as Holt's 8 pin stand-alone HI-8588 line receiver.

FEATURES

- Direct ARINC 429 interface to line driver and line receiver
- Both functions in a single 16 pin package
- Line Driver
  - Internal zener sets output levels
  - Digital output slope control
  - CMOS/TTL logic pins
- Line Receiver
  - Input hystersis at least 2 volts
  - Test inputs bypass analog inputs
  - Power down & output tri-state mode
- Plastic thermally enhanced surface mount (SO) package
- Mil-temperature range available

PIN CONFIGURATION



SUPPLY VOLTAGES

Vcc = +5V ± 5%
V+ = 12V to 15V
V- = -12V to -15V

PIN DESCRIPTION TABLE

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	V+	POWER	+12 TO + 15 VOLTS
2	TESTB	LOGIC INPUT	CMOS
3	ROUTB	LOGIC OUTPUT	RECEIVER CMOS OUTPUT B
4	ROUTA	LOGIC OUTPUT	RECEIVER CMOS OUTPUT A
5	TXBOUT	ARINC OUTPUT	LINE DRIVER TERMINAL B
6	TXAOUT	ARINC OUTPUT	LINE DRIVER TERMINAL A
7	N/C	NO CONNECT	
8	V-	POWER	-12 TO -15 VOLTS
9	GND	POWER	GROUND
10	TX1IN	LOGIC INPUT	CMOS OR TTL
11	TX0IN	LOGIC INPUT	CMOS OR TTL
12	RINA	ARINC INPUT	RECEIVER A INPUT
13	RINB	ARINC INPUT	RECEIVER B INPUT
14	TESTA	LOGIC INPUT	CMOS
15	SLP1.5	LOGIC INPUT	CMOS OR TTL, V+ IS OK
16	VCC	POWER	+5 VOLT SUPPLY