FINAL COM'L:-10 IND:-20

PALLV16V8-10 & PALLV16V8Z-20

Low Voltage, Zero Power 20-Pin EE CMOS Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- Low-voltage operation, 3.3 V JEDEC compatible
  — V_{CC} = +3.0 V to +3.6 V
- Pin and function compatible with all 20-pin PAL® devices
- Electrically-erasable CMOS technology provides reconfigurable logic and full testability
- Direct plug-in replacement for the PAL16R8 series
- Designed to interface with both 3.3-V and 5-V logic
- Outputs programmable as registered or combinatorial in any combination
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power up
- Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages
- Extensive third-party software and programmer support
- Fully tested for 100% programming and functional yields and high reliability

GENERAL DESCRIPTION

The PALLV16V8 is an advanced PAL device built with low-voltage, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALLV16V8 will directly replace the PAL16R8, with the exception of the PAL16C1.

The PALLV16V8Z provides zero standby power and high speed. At 30-µA maximum standby current, the PALLV16V8Z allows battery powered operation for an extended period.

The PALLV16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

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