PRODUCT EVALUATION

OF THE

ZILOG Z80-CTC

125

MARY ANN CLINGAN

INTEGRATED CIRCUIT ENGINEERING CORPORATION
ELECTRONIC KNOW-HOW FOR INDUSTRY

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MARY ANN CLINGAN

June 12, 1979

Prepared by
INTEGRATED CIRCUIT ENGINEERING CORPORATION
6710 EAST CAMELBACK ROAD SUITE 211
SCOTTSDALE, ARIZONA 85251

10379-K

SUMMARY

The purpose of this analysis is to gain first-hand knowledge on physical and electrical structuring of this circuit. This permits identification of the strong and weak features of this device and isolation of areas requiring in-depth analysis. In this way, a basis will be provided for predicting circuit reliability and establishing a background for future analysis.

The Z80-Counter Timer Circuit (CTC) provides counting and timing functions for microcomputers based on the Z80-CPU. The four independent channels are programmable to operate as either a counter or a timer. This circuit requires a single 5-volt supply and a single-phase 5-volt clock. The Z80-CTC utilizes N-channel silicon-gate depletion-load MOS technology and is packaged in a 28-pin DIP. A priority interrupt structure that is dedicated to the Z80-CPU provides for automatic interrupt vectoring without external logic.

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INTRODUCTION

To evaluate the Zilog Z80 Counter-Timer-Circuit (CTC) a total of four parts were used. Two of these parts were received from a Zilog representative. These were engineering samples and were not used for any electrical testing. The remaining two devices were ordered from a local distributor and received within two weeks. These MOS devices were received inserted in conductive foam and boxed for static discharge protection.

The engineering samples received from the Zilog representative had no package markings. The devices received from the local distributor were marked with the Zilog logo, part number (Z80-CTC), date code (7714), and lot control number (08201). The devices were packaged in 28-pin ceramic dual-in-line packages having standard operating ranges of 5V $\pm$ 5% and 0°C to 70°C. The ceramic package and standard operating range were the only options available at the time the devices were ordered.

The two devices purchased from a local distributor were used for the physical analysis including X-ray, leak tests, gas analysis, package examination, internal visual and SEM inspection. The remaining mechanical samples were used only for circuit tracing.

SECTION I - EXTERNAL PACKAGE ANALYSIS

1.1 - Visual

The Z80-CTCs were packaged in 28-pin ceramic DIPs with Kovar gold-plated lids which were soldered on to provide a hermetic seal. Kovar gold-plated leads were side brazed to the package. Physical measurements were taken and compared with the package outline in the data sheet. All measurements were within the tolerances stated. Table 1-1 is a comprehensive listing of the external physical measurements.

Photographs of the Zilog Z80-CTC package (sample 2K) are provided in Figure 1-1.

1.2 - X-Ray

Sample 2K was X-rayed, and the results are shown in Figure 1-2. One edge of the die is unsupported, with no eutectic material visible. If the wire bonding operation takes place above the unsupported edge of the silicon, then microcracks can result. This hazard should be monitored as a reliability problem. The X-ray shows that the other three edges are adequately supported and have no excessive build-up of the eutectic material.

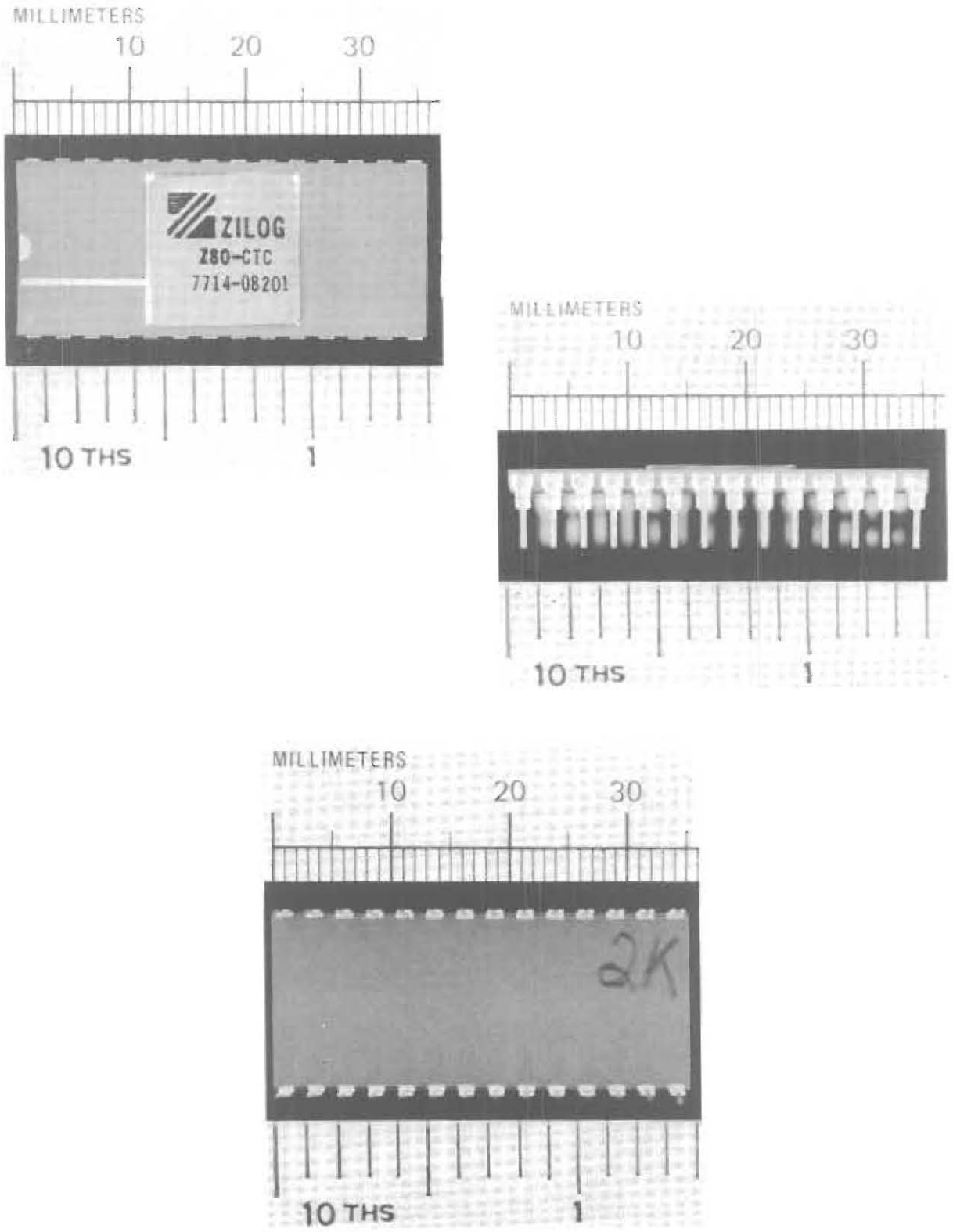
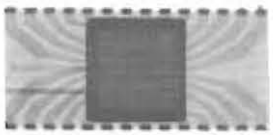


FIGURE 1-1. ZILOG Z80-CTC PACKAGE PHOTOGRAPHS.

TABLE 1-1

ZILOG Z80-CTC PACKAGE SPECIFICATIONS

PACKAGE DIMENSIONS:	L: 1.4" W: 0.59" TH: 0.082"
PACKAGE MATERIAL:	Dark Ceramic
LID DIMENSIONS:	L: 0.5" W: 0.5" TH: 0.01"
LID MATERIAL:	Kovar Gold-Plated
SEALING METHOD:	Soldered
LEAD SPACING:	0.59" x 0.08"
LEAD MATERIAL:	Kovar Gold-Plated
LEAD DIMENSIONS:	L: 0.13" W: 0.016" TH: 0.01"
LEAD ATTACHMENT METHOD:	Side Brazed
LEAD FRAME MATERIAL IN BONDING AREA:	Gold-Plated



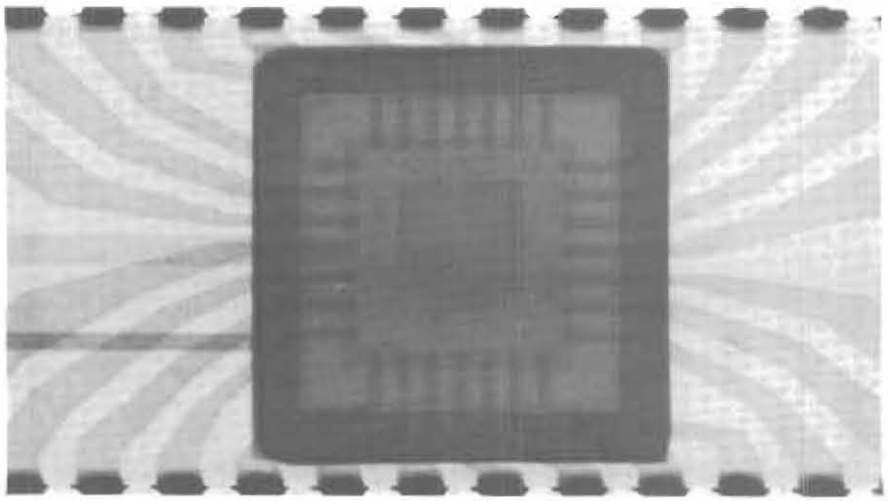


FIGURE 1-2. ZILOG Z80-CTC X-RAY PHOTOGRAPHS.

In the lead frame area, there are virtually no voids or any spacing problem with lead interconnect.

1.3 - Leak Test and Gas Analysis

Leak tests were performed on sample 2K per MIL-STD-883B, Method 1014.2, Conditions B and C. During both fine and gross leak tests, the part exhibited a leak rate of less than 1×10^{-8} atm cc/sec., the test limit.

Gas analysis was done on sample 2K per MIL-STD-883B Method 1018.1. The results of these tests are shown in Table 1-2. The moisture content was 0.09%, which is judged to be a safe level. The water vapor should be no greater than 0.5%, and ideally less than 0.1%. Gas analysis results would imply that these circuits were sealed in a dry nitrogen atmosphere.

TABLE 1-2

GAS ANALYSIS OF THE Z80-CTC SAMPLE 2K

CONSTITUENT	CONCENTRATION (%VOL/VOL)
ARGON (Ar)	0.44
HYDROGEN (H_2)	0.57
NITROGEN (N_2)	98.9
WATER VAPOR (H_2O)	0.09

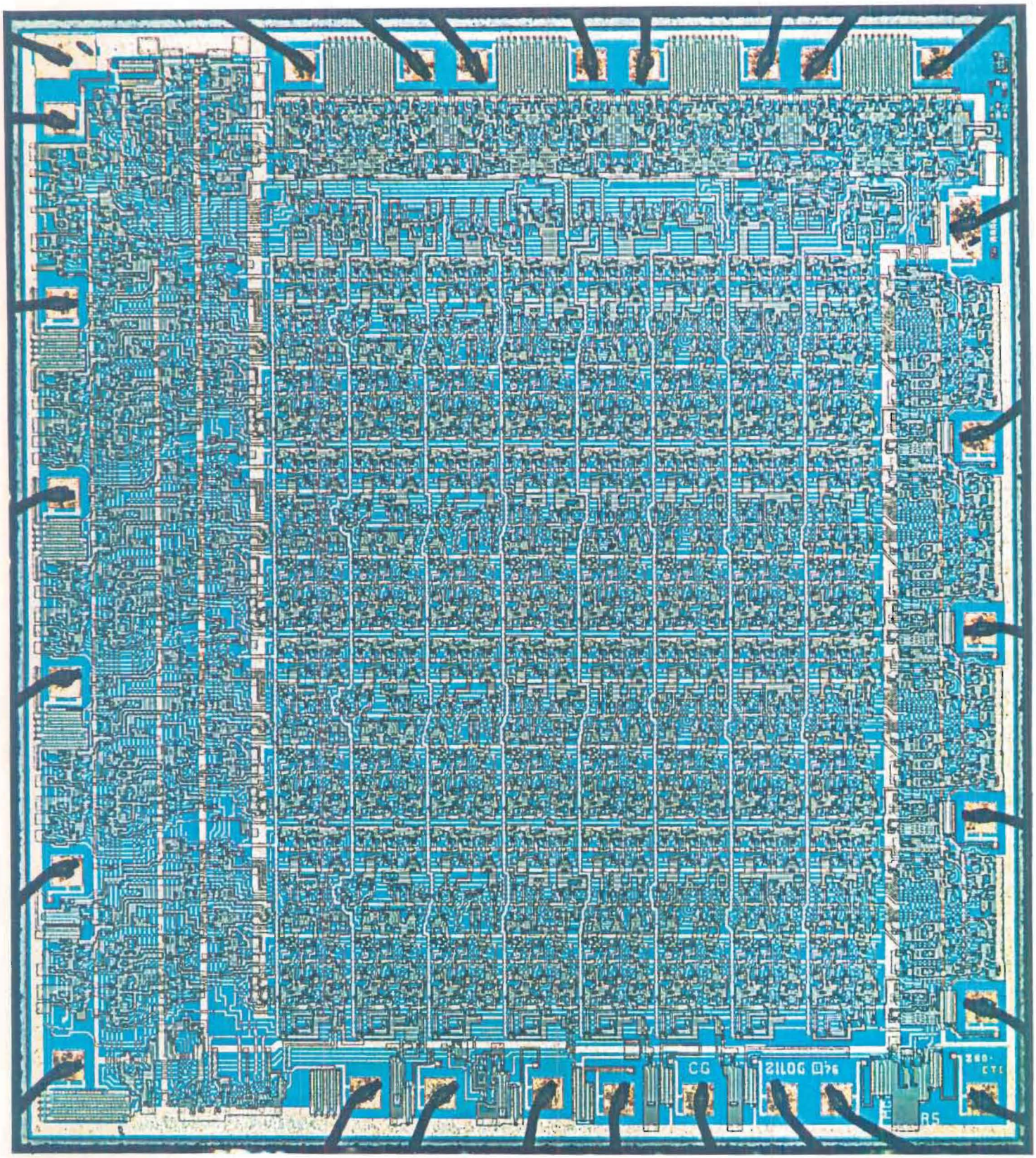
SECTION II - INTERNAL PACKAGE ANALYSIS

The lid of the Zilog Z80-CTC (sample 2K) was mechanically removed and the die cavity inspected according to the procedures prescribed in MIL-STD-883B, Method 2010.3, Test Condition B. This is not a comparison to MIL-STD's but this MIL-STD provides a detailed inspection procedure.

Figure 2-1 is a whole die photograph of the Z80-CTC. A view of the assembled die in the cavity is seen in the SEM photograph of the cavity area in Figure 2-2. There is a good fit between the circuit die and the cavity. Since the bonding pad layout on the die necessitates the use of a bonding wire 140 mils long, this should be an area of concern. Long bonding wires can sag and eventually cause a clearance problem between the bonding wire and the die. This would be most likely to occur under shock conditions. As seen in Figure 2-2, the wires are forward bonded, which does produce better clearance. Workmanship in the assembly area is good.

2.1 - Die Separation and Mounting

The Zilog Z80-CTC die was separated from adjacent die by the saw and break method as shown in in Figure 2-3. SEM inspection of sample 1K disclosed no chips or cracks along the edge of the die, nor cracks extending inward toward any active circuit element. A void under the die of sample 2K is shown in Figure 2-4. This is the same sample that was X-rayed and determined to be unsafe. Since there is a bonding pad above the unsupported silicon, the reliability hazard of microcracks does exist. Further observation in the SEM revealed no evidence of flaking, balling or excessive build-up of the eutectic material. Die



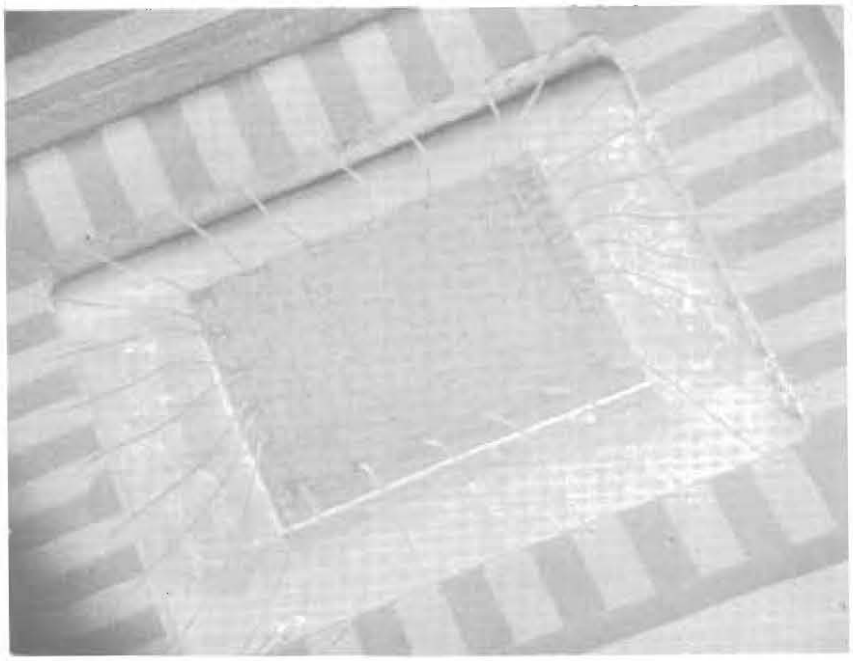
82X

FIGURE 2-1. ZILOG Z80-CTC WHOLE DIE PHOTOGRAPH.

TABLE 2-1
ZILOG Z80-CTC DIE SPECIFICATIONS

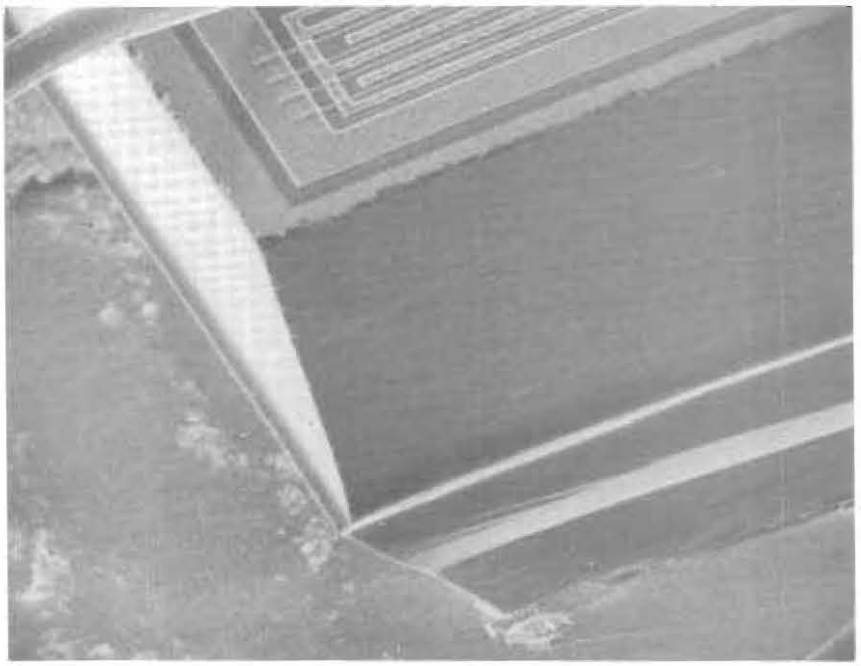
Cavity Size:	250 mils x 250 mils
Die Size:	90 mils x 135 mils
Area:	12,150 sq. mils
Thickness:	Approx. 15 mils
Die Separation Technique:	Saw and Break
Die Attach Method:	AuSi Eutectic
Wire Bonding Method:	Ultrasonic Wedge Bonding
Wire Bonding Material:	1.2 mil Aluminum Wire
Longest Span:	140 mils
Minimum Bonding Pad Size:	4.3 mils x 4.3 mils
Minimum Bonding Pad Window:	4.0 mils x 4.0 mils
Minimum Bonding Pad Spacing:	3.0 mils
Minimum Spacing Pad to Scribe:	4.0 mils
Minimum Spacing Pad to Nearest Metal Line:	1.3 mils
Minimum Contact Size:	0.3 mils dia.
Minimum Diffusion Spacing:	0.25 mils
Minimum Diffusion Width:	0.3 mils
Minimum Metal Line Width:	0.25 mils
Minimum Metal Line Spacing:	0.4 mils
Minimum Polysilicon Width:	0.25 mils
Minimum Polysilicon Spacing:	0.3 mils
Minimum Gate Size:	L: 0.25 mils W: 0.3 mils

Bond Strength Test 28 Wires
Average: 4.42 grams High: 5 grams Low: 3.5 grams Std. Dev: 0.44 grams
Die Shear Test: Did not shear at 2500 grams



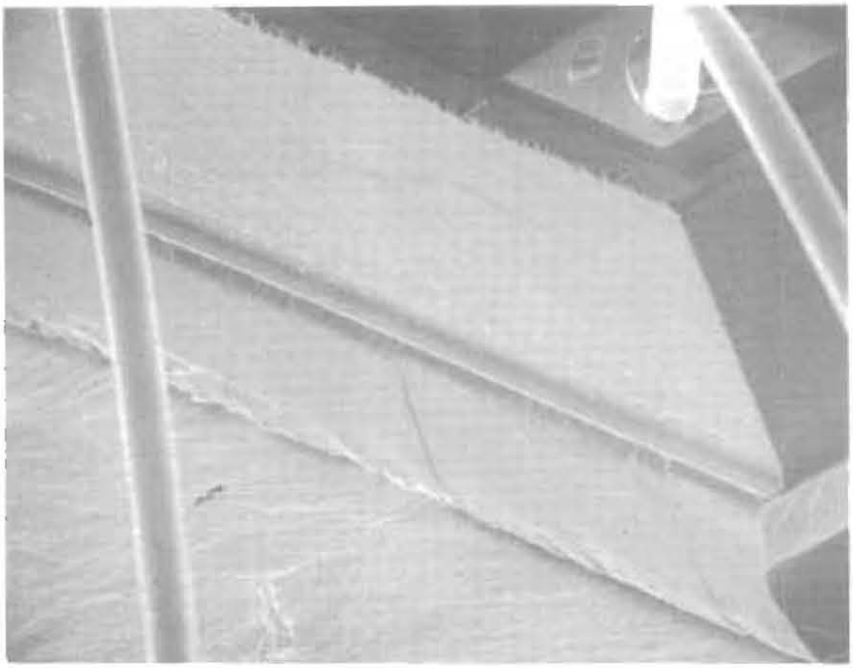
240X 55°

FIGURE 2-2. ZILOG Z80-CTC DIE CAVITY AREA.

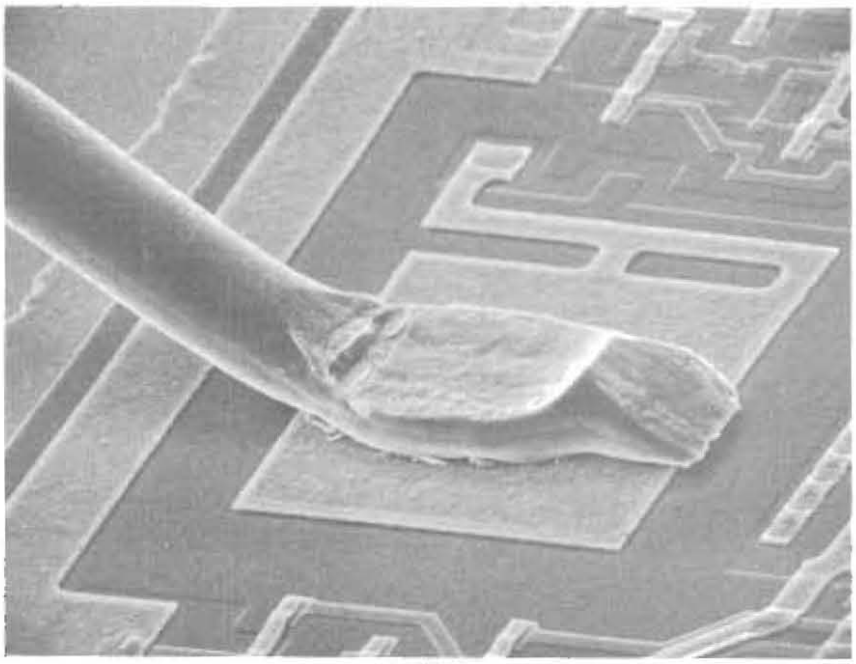


15X 45°

FIGURE 2-3. ZILOG Z80-CTC SAW AND BREAK DIE SEPARATION.



240X 65°



600X 55°

FIGURE 2-5. ZILOG Z80-CTC WIRE BOND.

shear testing was performed on sample 1K. The die did not shear at 2500 grams.

2.2 - Interconnection

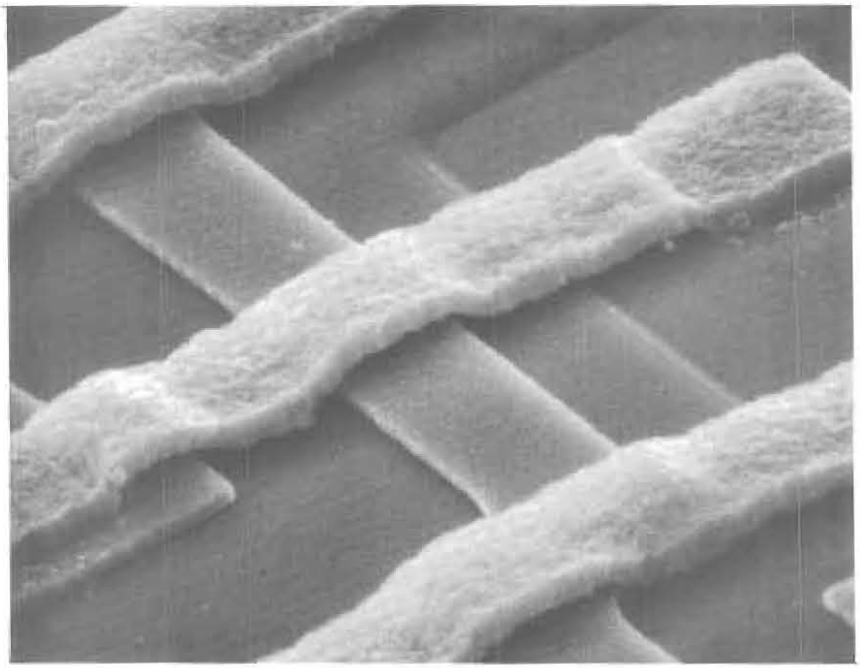
The Zilog Z80-CTC was interconnected by ultrasonic wedge bonding. A typical wedge bond is seen in Figure 2-5. The interconnection material was aluminum wire 1.2 mils in diameter. All bonds were inspected in the SEM and found to be adequate. The forward bonding technique was used on this device. Forward bonding provides good clearance between the wire and the circuit die.

Bond strength tests were done on sample 1K. The majority of failures were wire breaks at the neck down point; that is, the point at which the cross section of the wire is reduced due to the bonding process. The average pull strength was 4.42 grams. The lowest pull strength was 3.5 grams, well above the MIL-STD-883B Method 2011.2 minimum requirement of 2 grams for 1.2 mil wire.

2.3 - Examination of the Die Surface

Examination of the die surface was done on both sample 1K and 2K, first with the glassivation intact and then with glassivation removed. At both steps no anomalies were found. All spacings and line widths

appeared to be adequate for high yields and reliability concerns. An SEM photograph of metallization step coverage is shown in Figure 2-6. The step coverage was good and all contact holes were completely covered with metallization.



490X 55°

FIGURE 2-6. ZILOG Z80-CTC METAL STEP COVERAGE.

SECTION III - PROCESSING

The Zilog Z80-CTC was fabricated with an N-channel silicon-gate depletion-load MOS process using local oxidation to isolate adjacent diffusions. Table 3-1 presents the postulated processing sequence.

TABLE 3-1

POSTULATED PROCESS SEQUENCE FOR THE ZILOG Z80-CTC

STARTING MATERIAL: HIGH RESISTIVITY P-TYPE SUBSTRATE

STEP 1	GROW THIN OXIDE	
STEP 2	DEPOSIT NITRIDE	
STEP 3	APPLY PHOTORESIST AND PATTERN (FOR FIELD OXIDATION)	MASK 1
STEP 4	ETCH NITRIDE	
STEP 5	ION IMPLANT BORON (FIELD DOPING)	
STEP 6	GROW FIELD OXIDE	
STEP 7	STRIP NITRIDE AND UNDERLYING OXIDE	
STEP 8	GROW THIN OXIDE LAYER	
STEP 9	APPLY PHOTORESIST AND PATTERN (FOR DEPLETION LOADS)	MASK 2
STEP 10	ION IMPLANT	
STEP 11	APPLY PHOTORESIST AND PATTERN (FOR BURIED CONTACTS)	MASK 3
STEP 12	ETCH OXIDE FOR CONTACTS	
STEP 13	DEPOSIT POLY	
STEP 14	APPLY PHOTORESIST AND PATTERN (GATES AND INTERCONNECTS)	MASK 4
STEP 15	ETCH POLY AND EXPOSED GATE OXIDE	
STEP 16	DIFFUSE N+ (PHOSPHOROUS) TO FORM THE SOURCE AND DRAIN REGIONS	
STEP 17	DEPOSIT INTERMEDIATE OXIDE	
STEP 18	APPLY PHOTORESIST AND PATTERN (FOR METAL CONTACTS)	MASK 5
STEP 19	ETCH INTERMEDIATE OXIDE	
STEP 20	DEPOSIT ALUMINUM	
STEP 21	APPLY PHOTORESIST AND PATTERN (FOR INTERCONNECT ETC.)	MASK 6
STEP 22	ETCH ALUMINUM	
STEP 23	DEPOSIT GLASSIVATION	
STEP 24	APPLY PHOTORESIST AND PATTERN (FOR BONDING PAD OPENINGS)	MASK 7
STEP 25	ETCH GLASSIVATION	

SECTION IV - CIRCUIT AND LOGIC ANALYSIS

4.1 - Die Partitioning

The Z80 Counter-Timer-Circuit (CTC) is divided into four independent programmable channels that provide counting and timing functions for the Z80-CPU. Figure 4-1 shows the channels across the middle of the chip. The layout is generally very compact with little wasted space. The bidirectional data bus is at the top, and the internal data bus runs vertically through the interrupt vector register, interrupt control logic and the counter/timer channels. Data bus latches are at the end of the internal data bus at the bottom of the chip. The four clock/trigger inputs are at the right edge with associated control circuitry. The three zero count/timeout outputs are along the left side with the channel interrupt logic. Read/Write control surrounds the $\overline{RD}$ input. The remaining interrupt and control lines enter the chip along the bottom edge. Two channel select lines enter at the lower right corner and are decoded in each channel.

V_{SS} (ground) enters the chip at the upper left corner. There are a few ground crossunders, but none that are connected to output driver circuits. With a total V_{SS} metal width of 3.5 mils, the average current density is about 35 mA/mil. V_{CC} enters the chip from the upper right corner with a wide metal run extending down the right side. The unbuffered clock enters the chip from the middle of the bottom edge and is distributed along both sides of the chip.

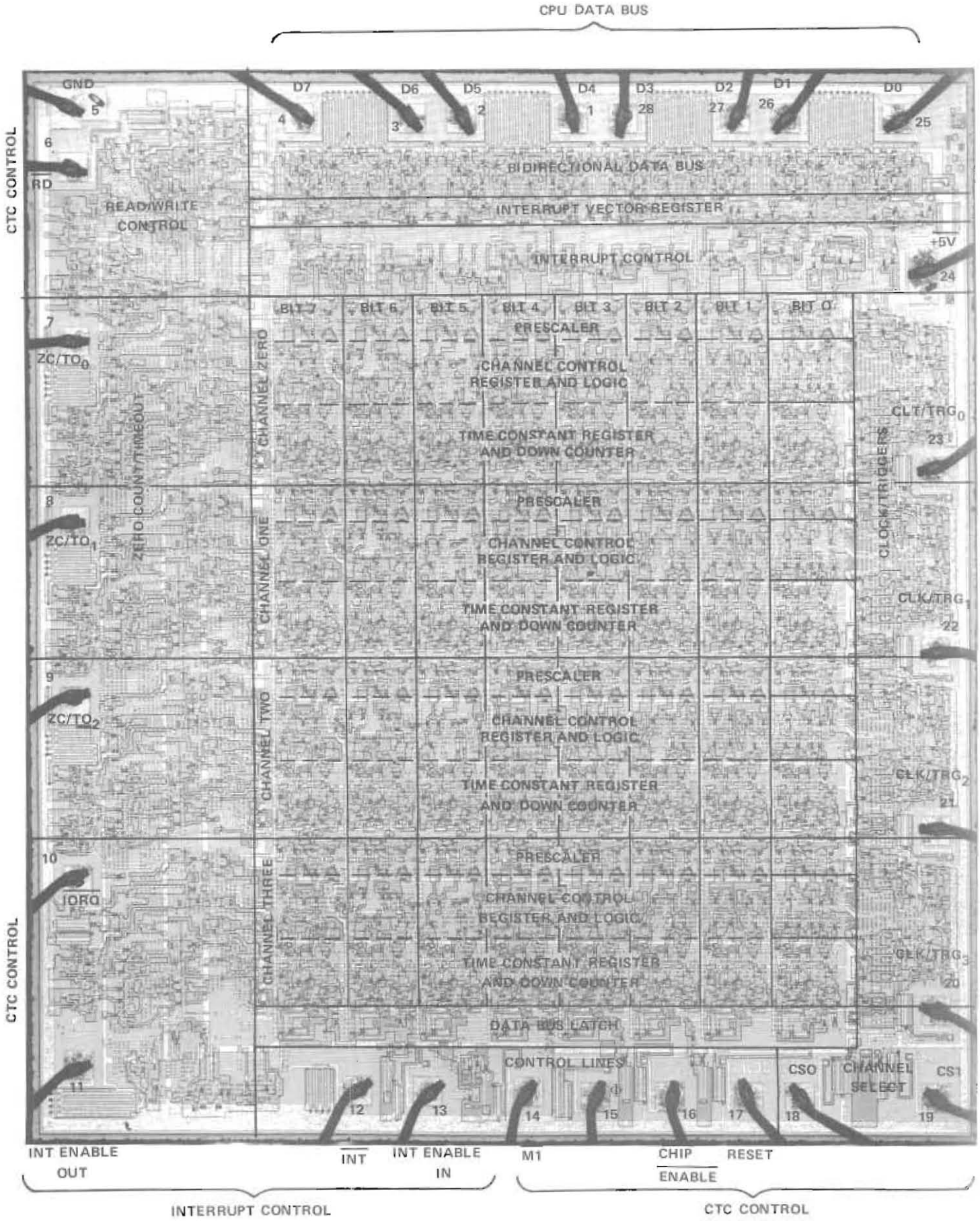


FIGURE 4-1. ZILOG Z80-CTC DIE PARTITIONING.

4.2 - Read/Write ($\overline{CE}$, $\overline{M1}$, $\overline{IORQ}$, and $\overline{RD}$ Inputs).

The circuitry illustrated in Figures 4-2 through 4-5 is part of the internal control logic block shown in Figure 1 (CTC Block Diagram) of the Z80-CTC product specification. This logic controls the transfer of data and control words between the Z80-CPU and the CTC.

Figure 4-2 illustrates a type-D flip-flop that is used throughout the CTC circuitry. The state of the Data ($\overline{D}$) input is transferred to the outputs (Q and $\overline{Q}$) on the rising edge of the Clock (C) input signal. The Reset (R) input makes Q "low" and $\overline{Q}$ "high". A logic block will be used to represent this circuit in the remaining schematics. In some flip-flops the connections to the inverter formed by transistors 1 and 2 are reversed, thus changing the $\overline{D}$ input to a D input. In other flip-flops the C input is complemented by reversing the two latches of the flip-flop. Data is then transferred on the falling edge of the Clock ($\overline{C}$) input. A schematic of a complex gate is shown formed by transistors 7 through 11.

Figure 4-3 illustrates the use of this flip-flop (FF1) in the Machine Cycle 1 ($\overline{M1}$) input. The $\overline{M1}$ signal originates in the Z80-CPU and indicates that the current machine cycle is an op code fetch cycle. The NOR gate latch and output driver composed of transistors 6 through 17 insure that transitions of $\overline{M1}$ will occur when Clock is "low." FF1 fully synchronizes $\overline{M1D}$ to the rising edge of Clock.

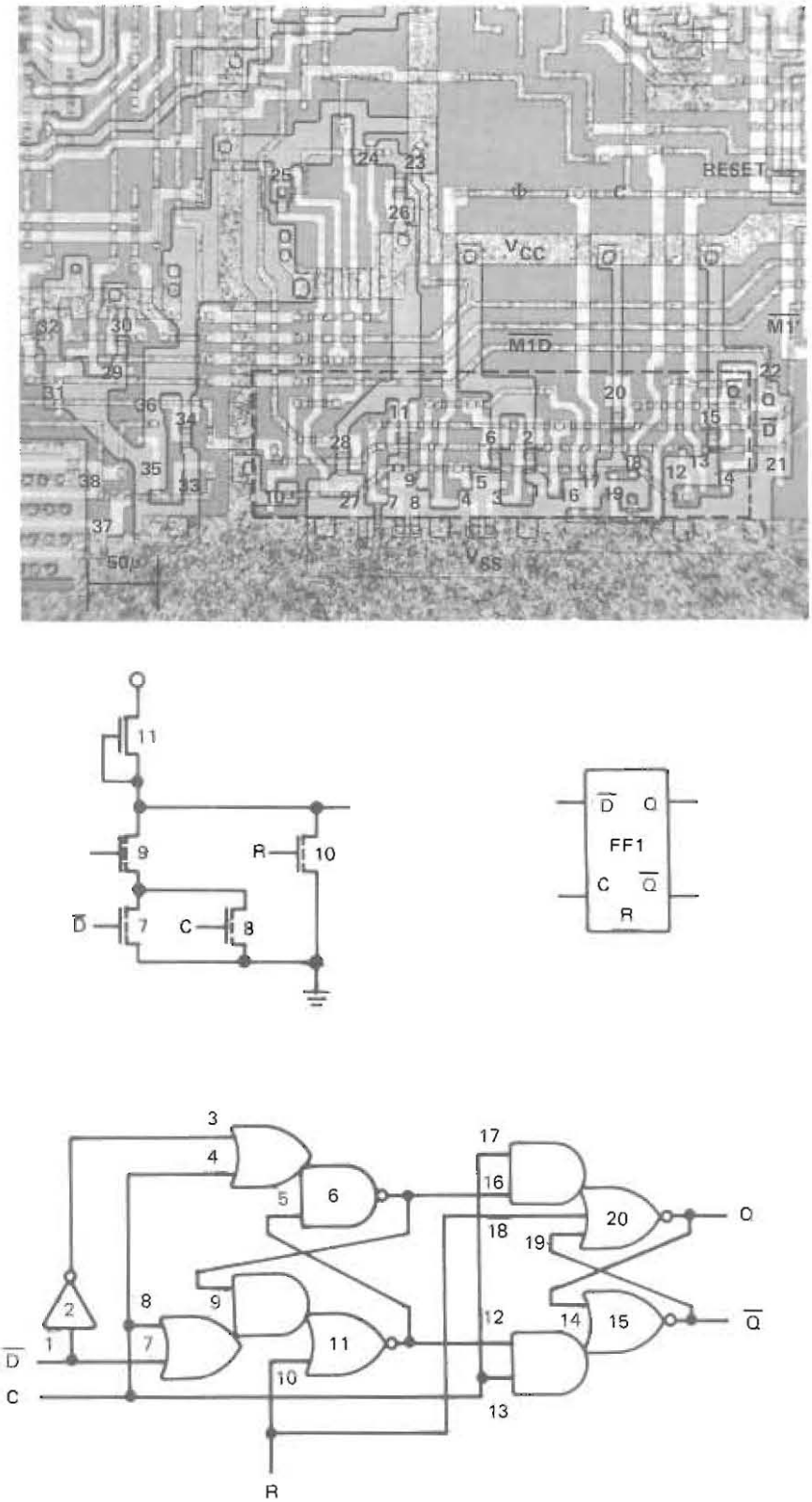
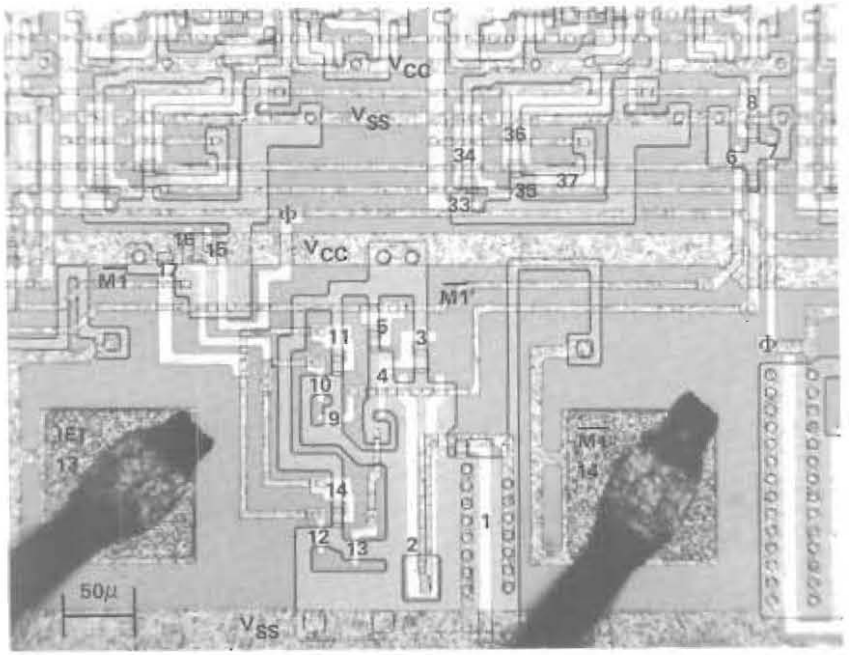
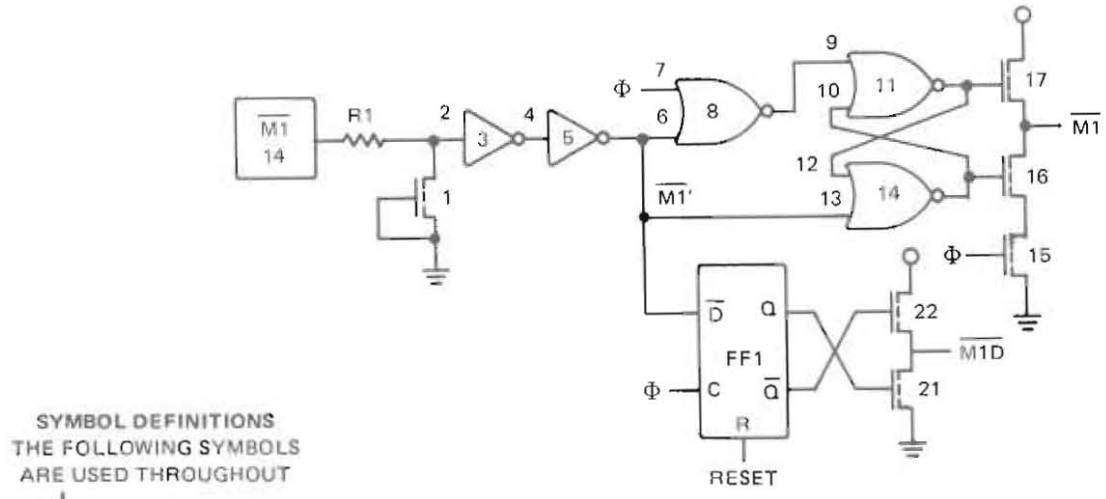


FIGURE 4-2. ZILOG Z80-CTC INTERRUPT ENABLE OUTPUT (IEO) AND TYPE D FLIP FLOP.





SYMBOL DEFINITIONS
THE FOLLOWING SYMBOLS
ARE USED THROUGHOUT

= ENHANCEMENT MODE TRANSISTOR

= DEPLETION MODE TRANSISTOR

= V_{CC}

= V_{SS} (GROUND)

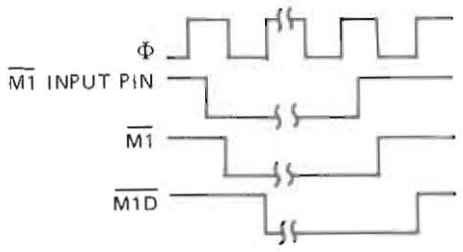


FIGURE 4-3. ZILOG Z80-CTC MACHINE CYCLE ONE ($\overline{M1}$) INPUT.

Figure 4-4 illustrates the circuitry used in transferring data from the CTC to the CPU. The four input NOR gate formed by transistors 8 through 12 detects a CPU read cycle. The $\overline{\text{READ REG}}$ signal is "low" whenever the CPU reads the current contents of the Down Counter.

Another CTC to CPU data transfer occurs during the interrupt acknowledge cycle. The NOR gate composed of transistors 72 through 76 (Photographed in Figure 4-5A) detects $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ "low" when there is a CTC interrupt active and Interrupt Enable In ($\overline{\text{IEI}}$) is "low".

Transistors 15 through 20 enable the data bus output drivers during a read cycle or an interrupt acknowledge cycle.

The four input NOR gate composed of transistors 77 through 81 detects a possible interrupt acknowledge cycle when $\overline{\text{M1}}$ is "low" while $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ are "high". FF2 synchronizes this signal to the leading edge of Clock. $\overline{\text{READ VECTOR}}$ places the interrupt vector onto the internal data bus. The vector is read by the CPU only when $\overline{\text{OUT}}$ is active.

Figures 4-5A and 4-5B illustrates the circuitry controlling data transfers to the CTC either from the CPU during a write cycle or program memory during a return from interrupt cycle.

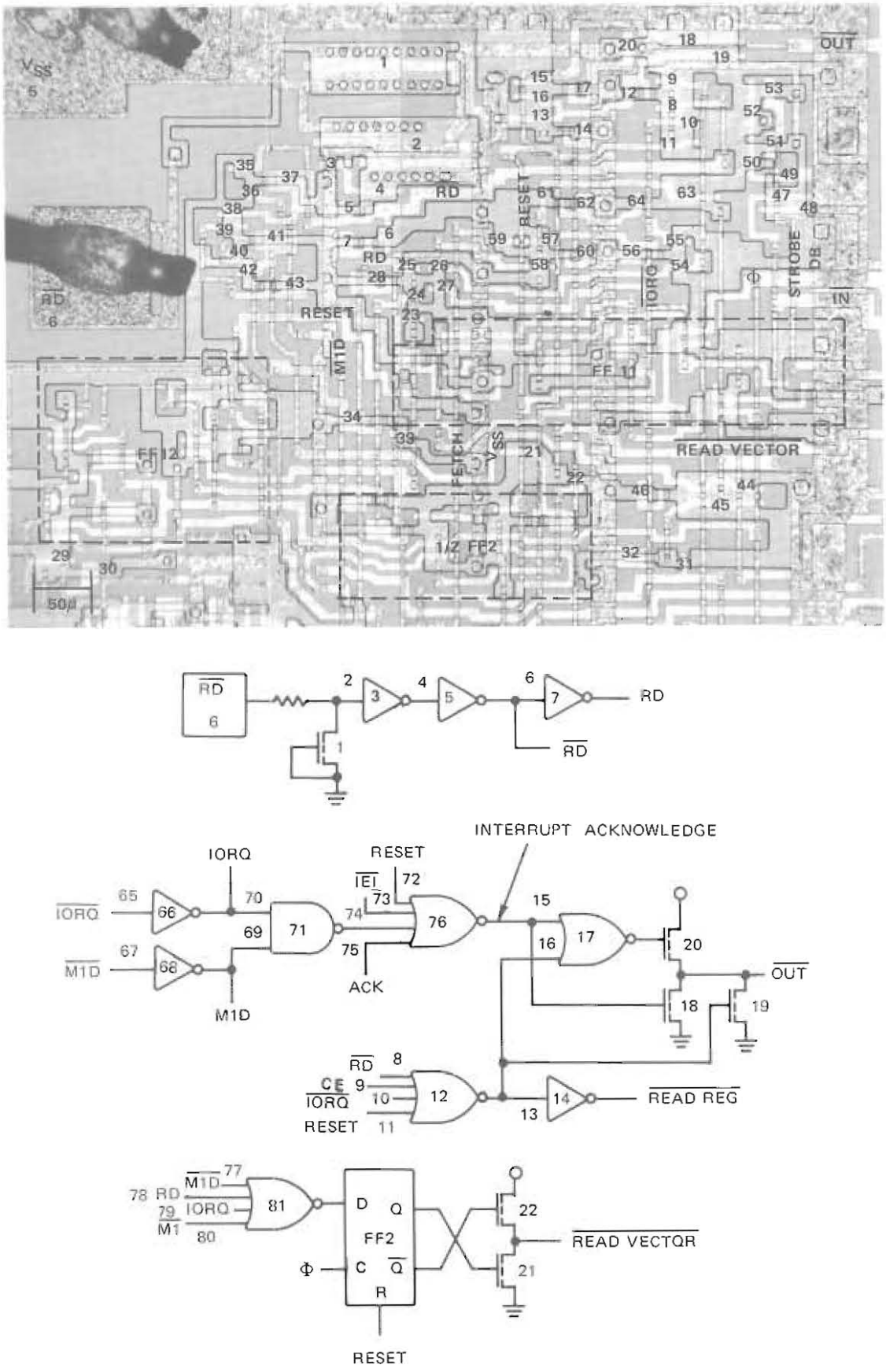
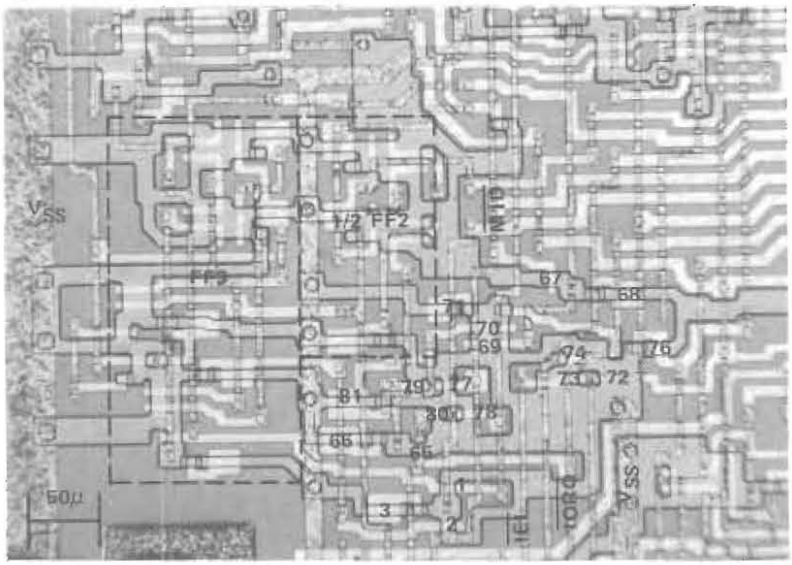


FIGURE 4-4. ZILOG Z80-CTC READ CYCLE STATUS ($\overline{RD}$) INPUT WITH READ CYCLE CIRCUITRY.



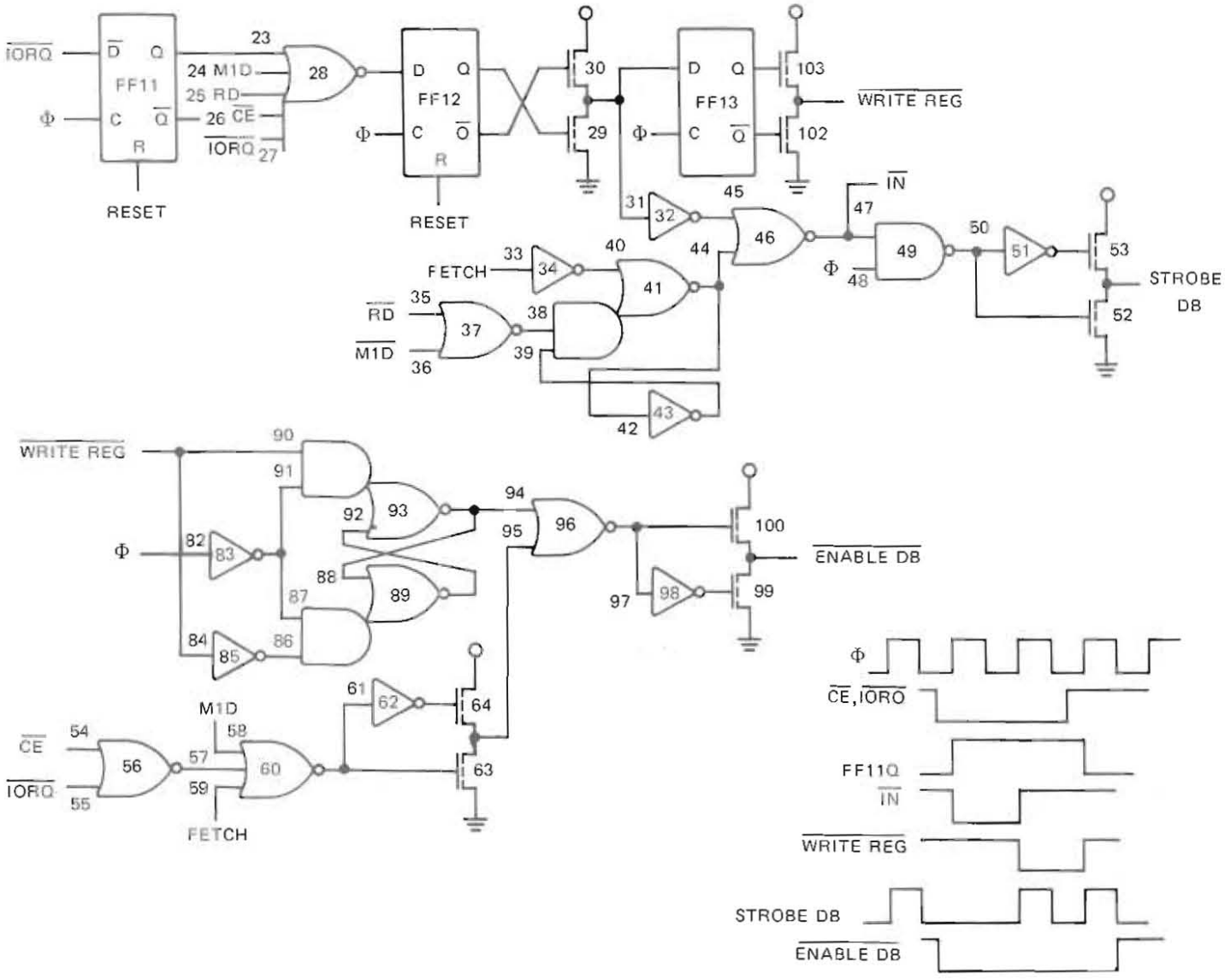
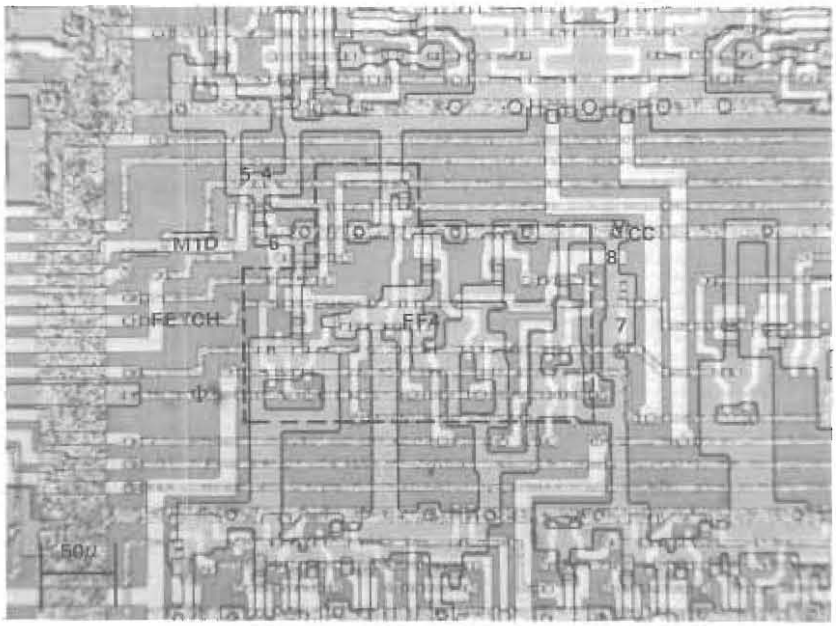
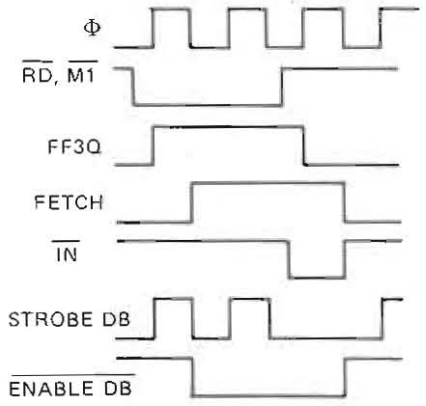


FIGURE 4-5A. ZILOG Z80-CTC WRITE CYCLE CIRCUITRY.





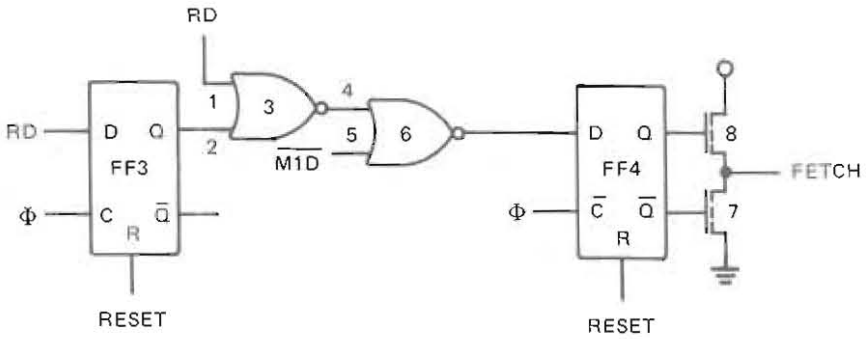


FIGURE 4-5B. ZILOG Z80-CTC WRITE CYCLE CIRCUITRY.

The combination of FF11 and the 5 input NOR gate (transistors 23 through 28) detect the beginning of a write cycle. The output of the NOR gate is "high" only until the next rising edge of Clock following a failling edge of $\overline{\text{IORQ}}$. Data is transferred to the CTC registers in two steps.

Data is transferred to the CTC registers in two steps.
First, external data is sampled by STROBE DB and transferred to the internal data bus by $\overline{\text{IN}}$. Then FF13 (photographed in Figure 4-7A) delays one full clock cycle and $\overline{\text{WRITE REG}}$ transfers internal data to the register latches.

During a return from interrupt cycle the CTC must decode the RETI instruction. FF3 and two NOR gates (Transistors 1 through 6) detect the beginning of an op code fetch cycle. FF4 delays this signal by one half clock time and generates the internal FETCH signal. Transistors 33 through 43 form a latch that accomplishes the two step data input function described earlier.

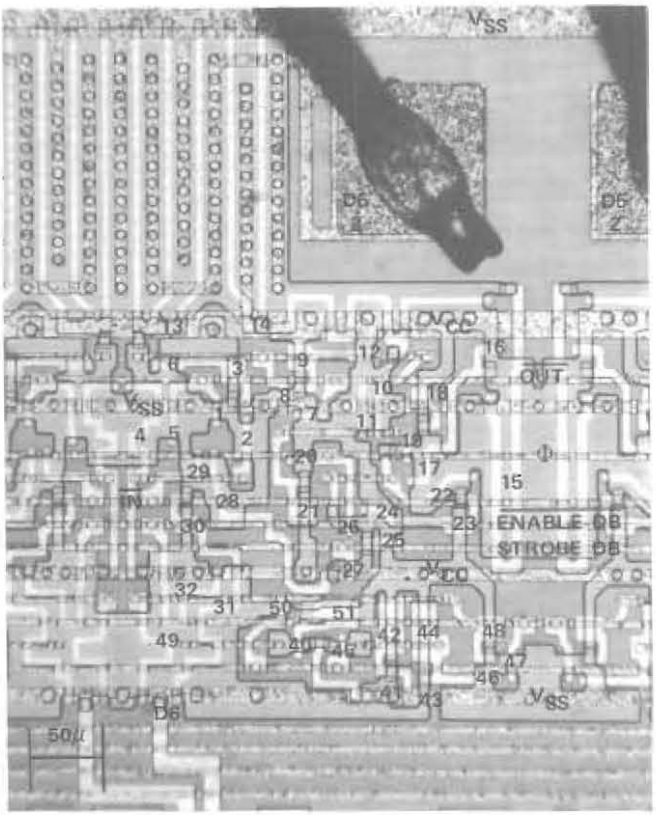
The $\overline{\text{ENABLE DB}}$ signal forces a logic "one" on the internal data bus whenever it is not being used for any data transfer function.
Transistors 54 through 64 detect all data bus transfers while the latch composed of transistors 82 through 93 (photographed in Figure 4-7A) extends the $\overline{\text{ENABLE DB}}$ signal by one half clock time at the end of a write cycle.

4.3 - Bidirectional Data Bus (D7 through D0)

Bit six of the Z80-CTC data bus buffer is illustrated in Figure 4-6. Transistors 1 through 14 form an output driver for the internal data bit D6. The driver circuit is enabled only when data is transferred from the CTC to the CPU. Otherwise, $\overline{OUT}$ is "high" and the driver is in a high impedance state. Data to be transferred to the CTC is first sampled by transmission gate 19 when Clock is "low". When Clock is "high", data is latched by transistors 22 through 26. Transmission gate 27 samples the latched data and transistors 29 through 31 drive the internal data bus during write or fetch cycles. Transistor 32 forces the internal data bus to a "high" state when it is not being used for data transfers. Transistors 33 through 37 (photographed in Figure 4-3) provide a latch for the data bus during the two step data transfers described in the previous section.

4.4 - Interrupt Servicing (IEI Input, $\overline{INT}$ and IEO Outputs).

The circuitry illustrated in Figure 4-7B decodes the RETI instruction used to reset CTC interrupts. The output of FF5 goes "high" after the first byte of any two byte instruction; that is, op codes CB_{16}, DD_{16}, ED_{16} or FD_{16}. If the op code is ED_{16}, then FF6 changes state and $\overline{ED}$ goes "low". This enables the circuitry that decodes the $4D_{16}$ op code (Transistors 48 through 57). The RETI signal will go "high" after the rising edge of the $\overline{RD}$ input ($\overline{IN}$=0) and will go "low" after the falling edge of FETCH.



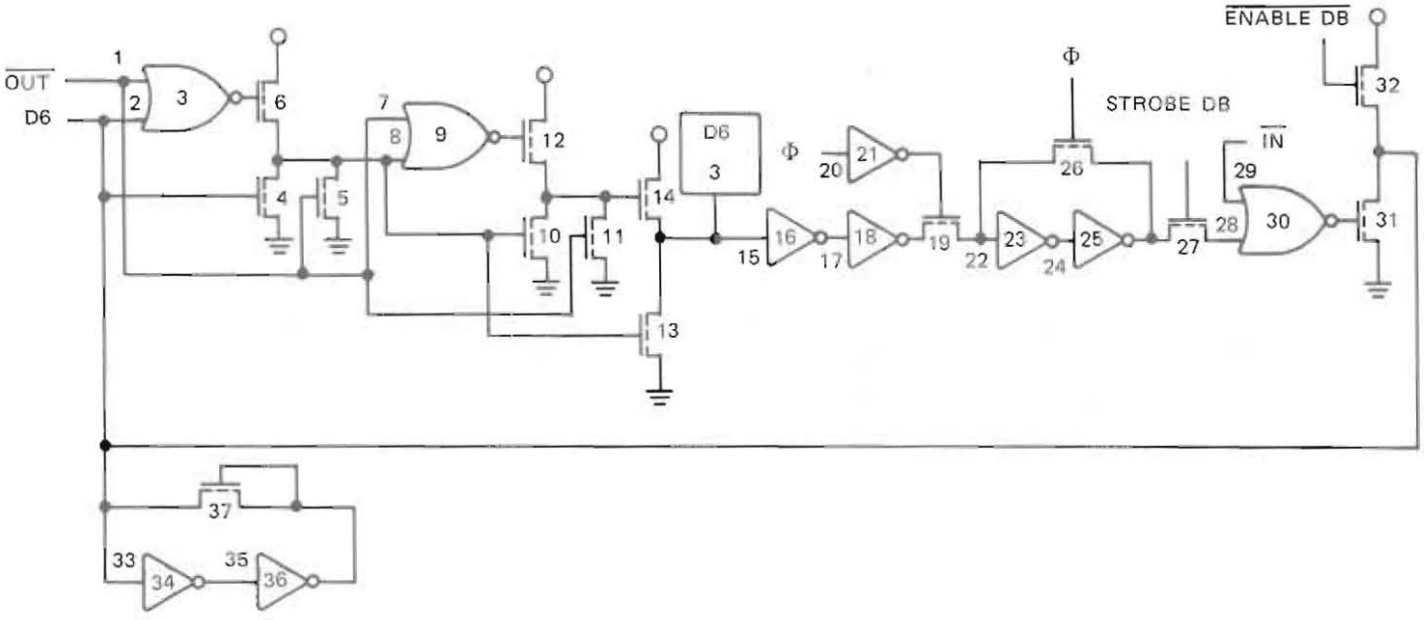


FIGURE 4-6. ZILOG Z80-CTC BIDIRECTIONAL DATA BUS (D6).

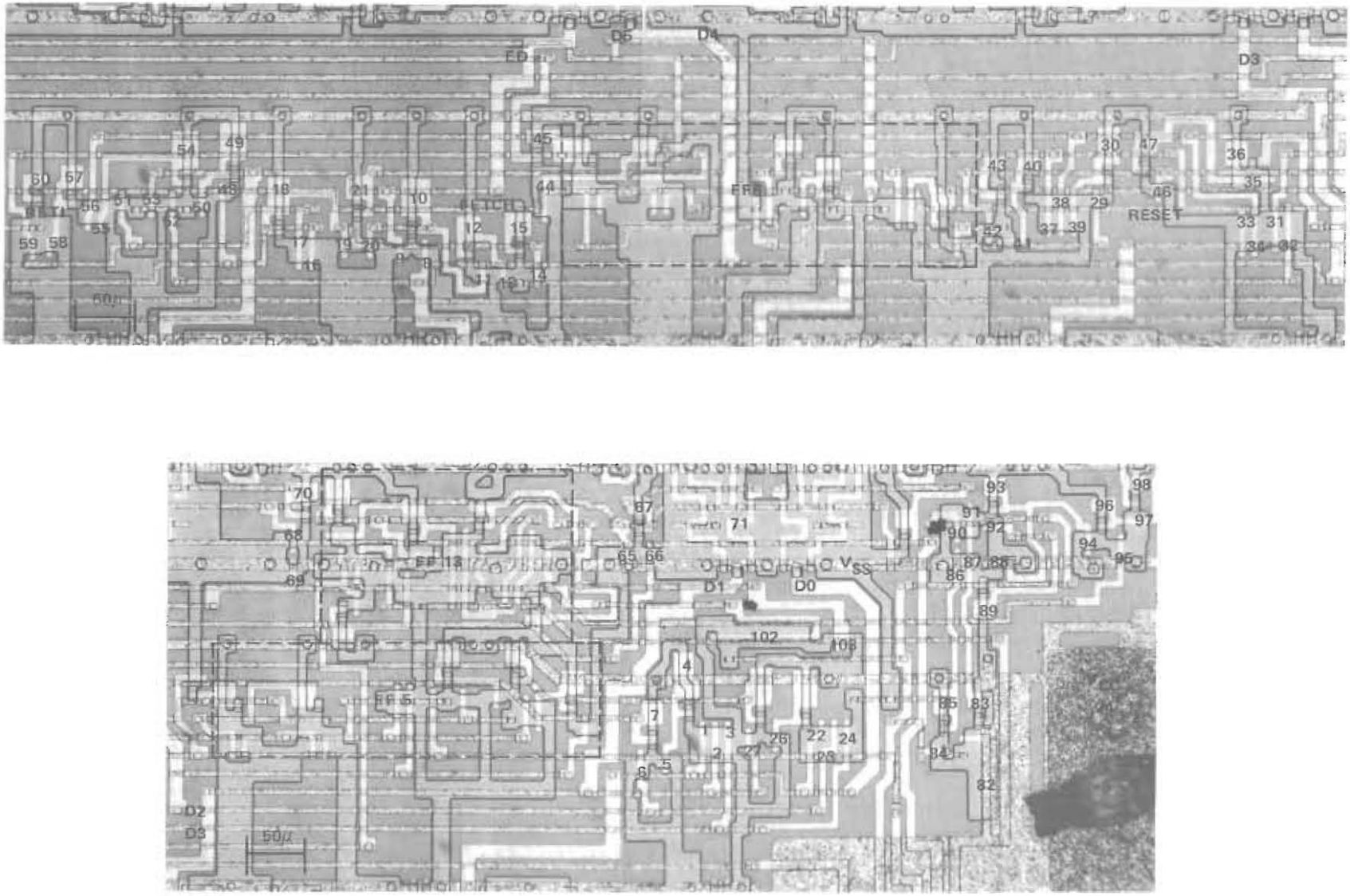


FIGURE 4-7A. ZILOG Z80-CTC RETURN FROM INTERRUPT INSTRUCTION DECODE.

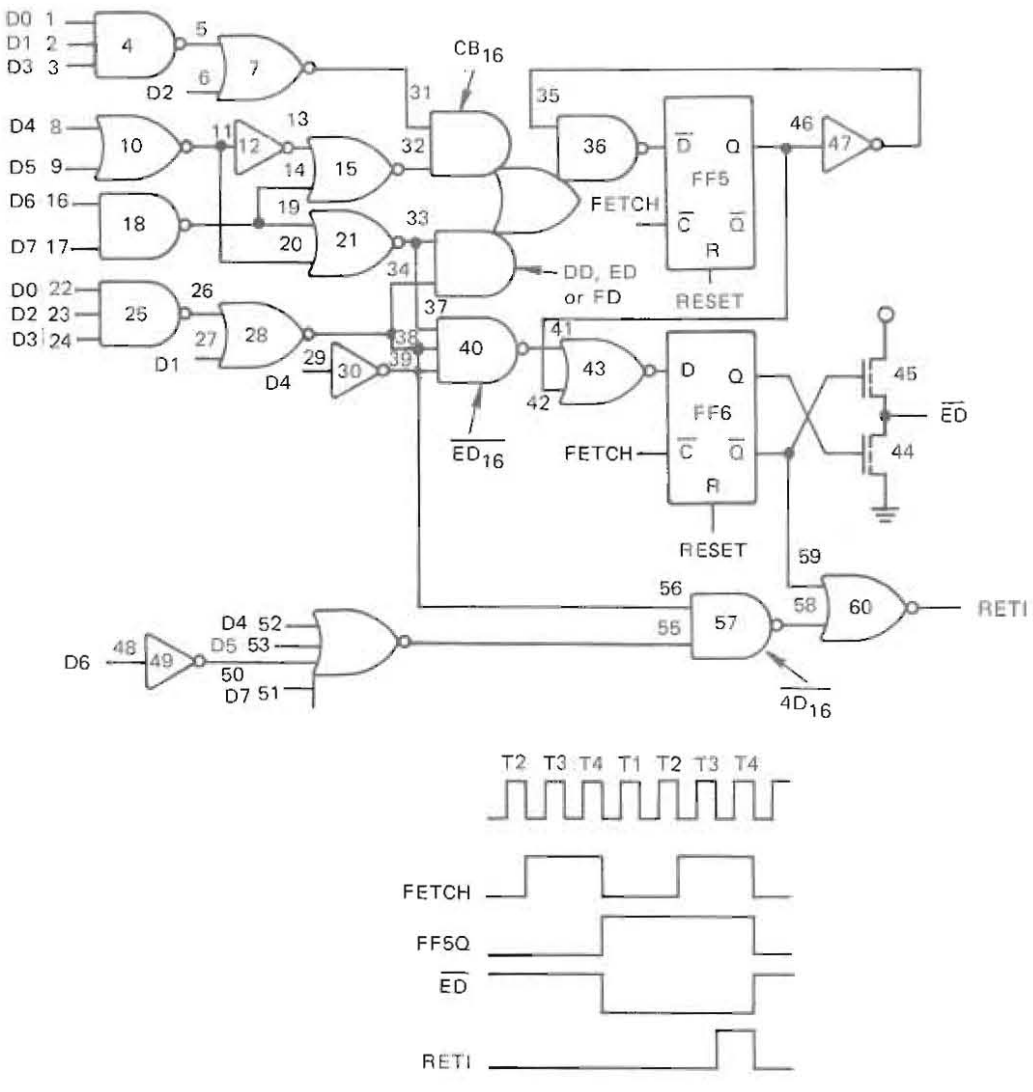


FIGURE 4-7B. ZILOG Z80-CTC RETURN FROM INTERRUPT INSTRUCTION DECODE.

Interrupt Enable In (IEI) and Interrupt Enable Out (IEO) form a system daisy chain for interrupts in which the device closest to the CPU has the highest priority. Within the CTC, interrupt priority is determined by channel number with channel zero having highest priority. When IEI is "high", no other interrupting devices of higher priority in the daisy chain are being serviced by the CPU.

The CTC interrupt circuitry is shown in Figure 4-8. Each channel (CHØ, 1, 2, and 3) has four outputs indicating the channel status to the priority interrupt system. IEI signals form the daisy chain within the CTC. Section 4.10 describes the channel interrupt logic.

When a channel down counter reaches zero, the CPU receives an Interrupt Request ($\overline{INT}$ = 0) from one or more of the channels and sends an Interrupt Acknowledge signal ($\overline{M1}$ + $\overline{IORQ}$ = 0). The interrupt pending (IP) signal inhibits acknowledgement of lower priority interrupts.

The highest priority interrupt requestor (the one with $\overline{IEI}$ = 0) places its interrupt vector on the data bus (ACK = 1, $\overline{READ\ VECTOR}$ = 0) and sets its interrupt-under service latch (IUS = 1).

The Z80-CPU executes a two byte RETI (RETurn from Interrupt) instruction at the end of an interrupt service routine. This instruction is decoded by the CTC and is used to reset the interrupt-under-service latch. The normal daisy chain operation can be used to detect a pending interrupt (IP=1). When the first byte (ED_{16}) of a two byte instruction is decoded ($\overline{ED}$ = 0), the daisy chain is modified by inhibiting all pending interrupts so that the device presently under service is the only one with IEI = 1 and IEO = 0.

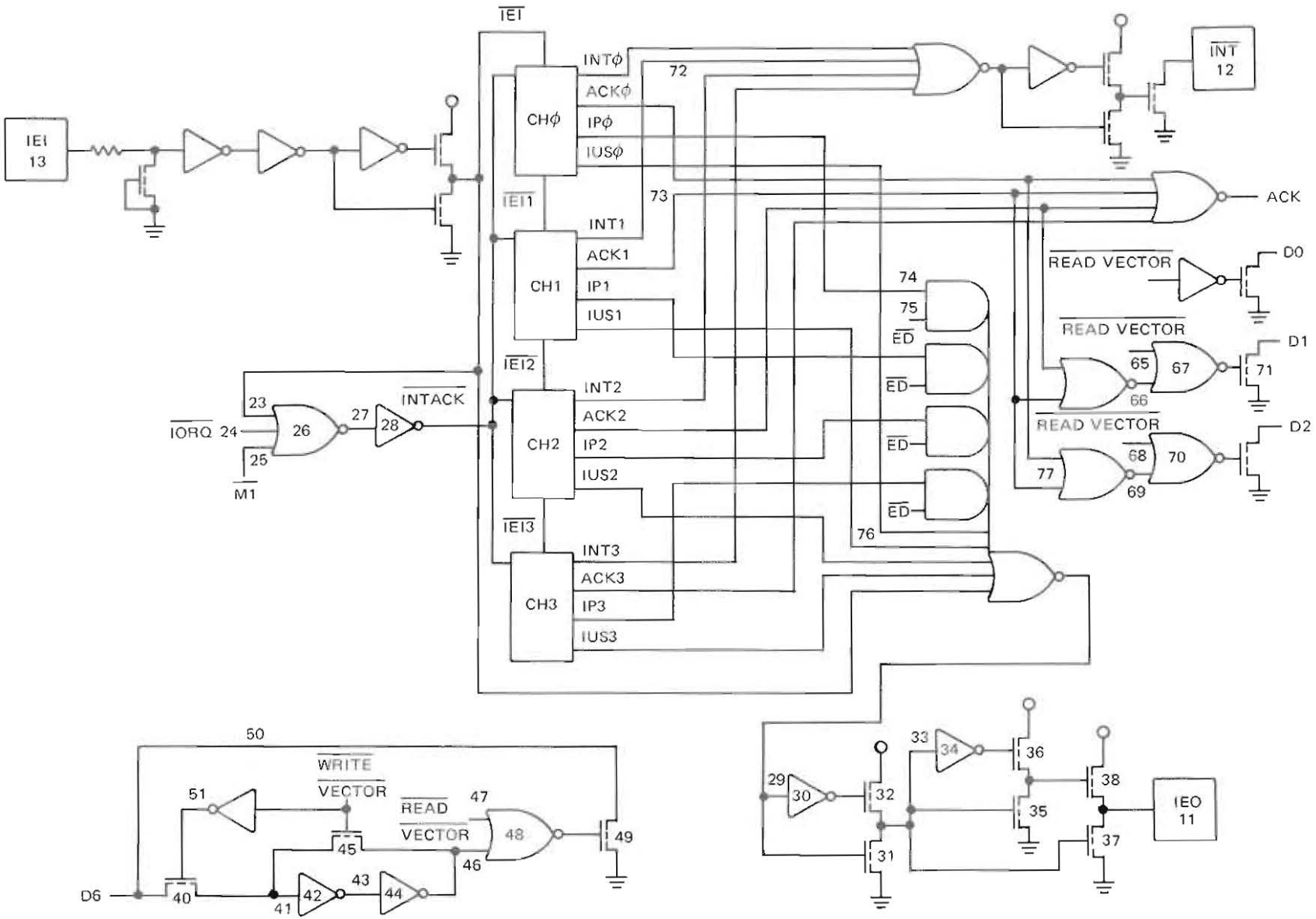


FIGURE 4-8. ZILOG Z80-CTC IEI INPUT AND $\overline{INT}$, IEO OUTPUTS WITH PRIORITY INTERRUPT.

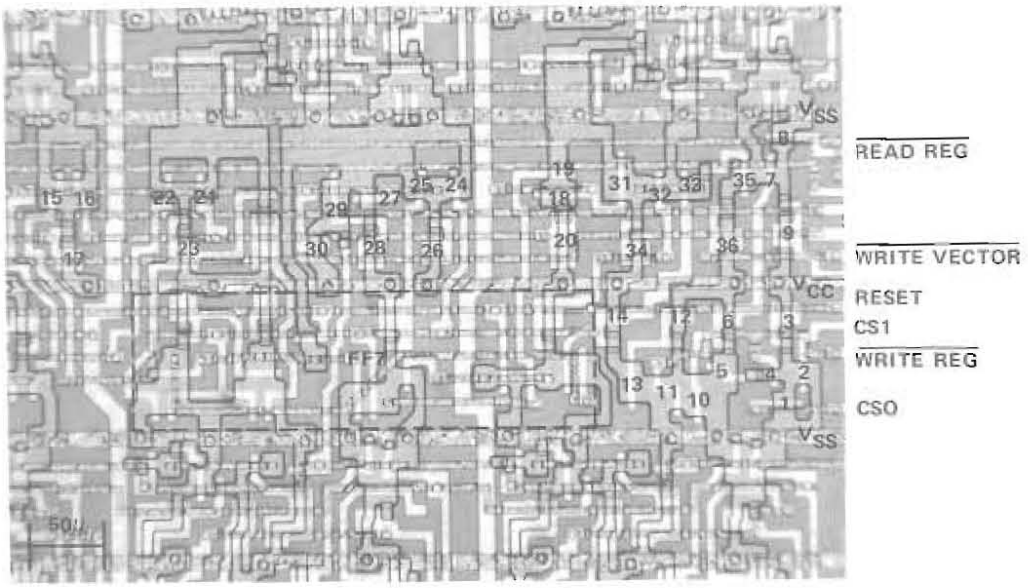
If the next byte is $4D_{16}$, the interrupt-under-service latch is reset (IUS = 0).

4.5 - Channel Select (CS1 and CS0 Inputs)

These inputs select one of four CTC channels for writing the channel control register (CCR) or time constant register (TCR) and reading the down counter (DC). The channel read/write circuitry of Figure 4-9 is part of the channel control logic block of Figure 2 (Channel Block Diagram) in the Z80-CTC specification. Channel zero generates $\overline{\text{WRITE VECTOR}}$ which loads an interrupt vector when D0=0. $\overline{\text{READ REG}}$ and $\overline{\text{WRITE REG}}$ are generated by the Read/Write circuitry discussed in Section 4.2. $\overline{\text{READ DC}}$ is synchronized to the rising edge of clock by FF19. WRITE TC is enabled by FF7 if, in the previous write to channel zero, D0 · D2 = 1.

4.6 - Channel Control Register

Each of the four channel control registers (CCR) select operating modes and conditions for a CTC channel. CS0 and CS1 are used to form a two bit binary address to select one of the channels. CCR bits 0 and 2 are associated with the channel READ/WRITE circuitry and are discussed in the previous section. Figures 4-10A and 4-10B illustrate CCR bits D1 and D3 through D7. Bits D4 through D7 are stored conditions and have latches on each bit. INTENA (bit 7) is initialized by reset so that no CTC channel can interrupt after RESET. Bit 1 (Reset Channel) resets FF8



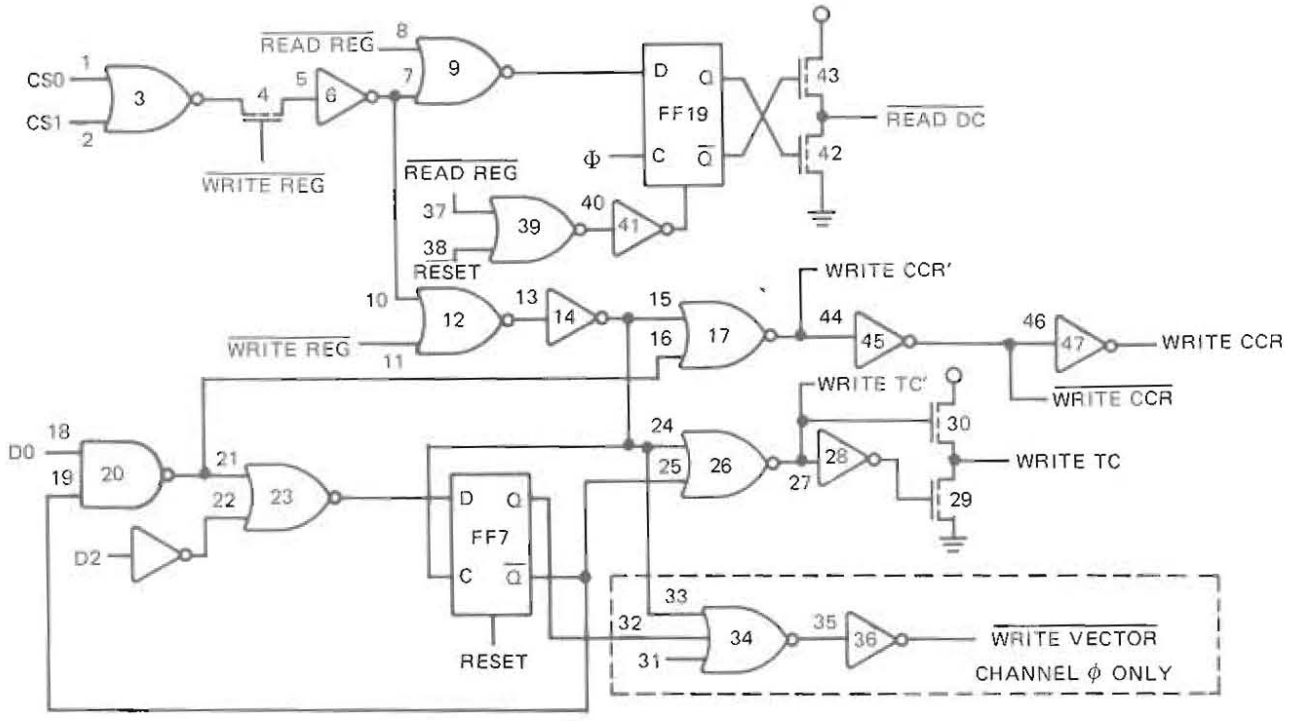


FIGURE 4-9. ZILOG Z80-CTC READ/WRITE CIRCUITRY (CHANNEL ϕ).

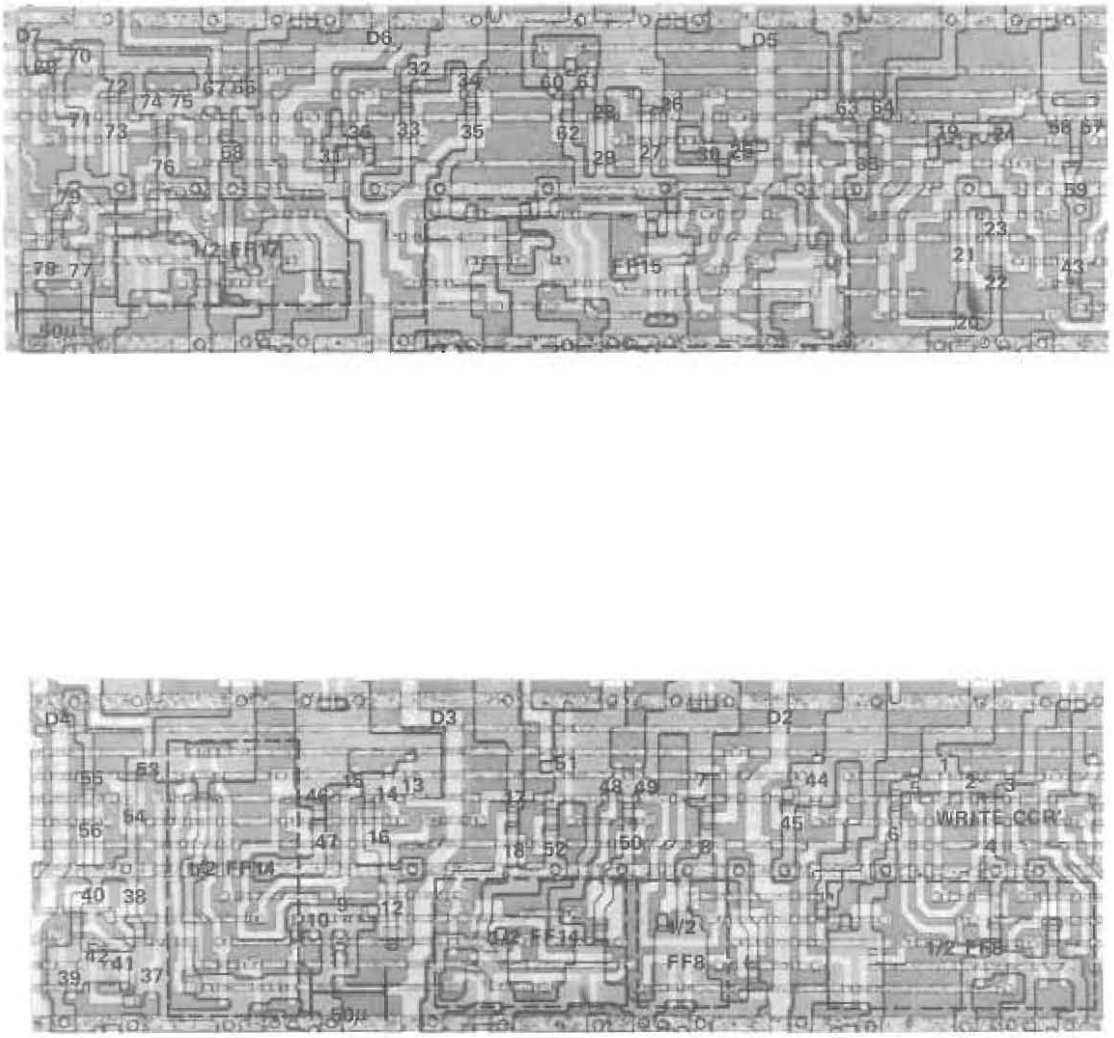


FIGURE 4-10A. ZILOG Z80-CTC CHANNEL CONTROL REGISTER (CHANNEL ϕ).

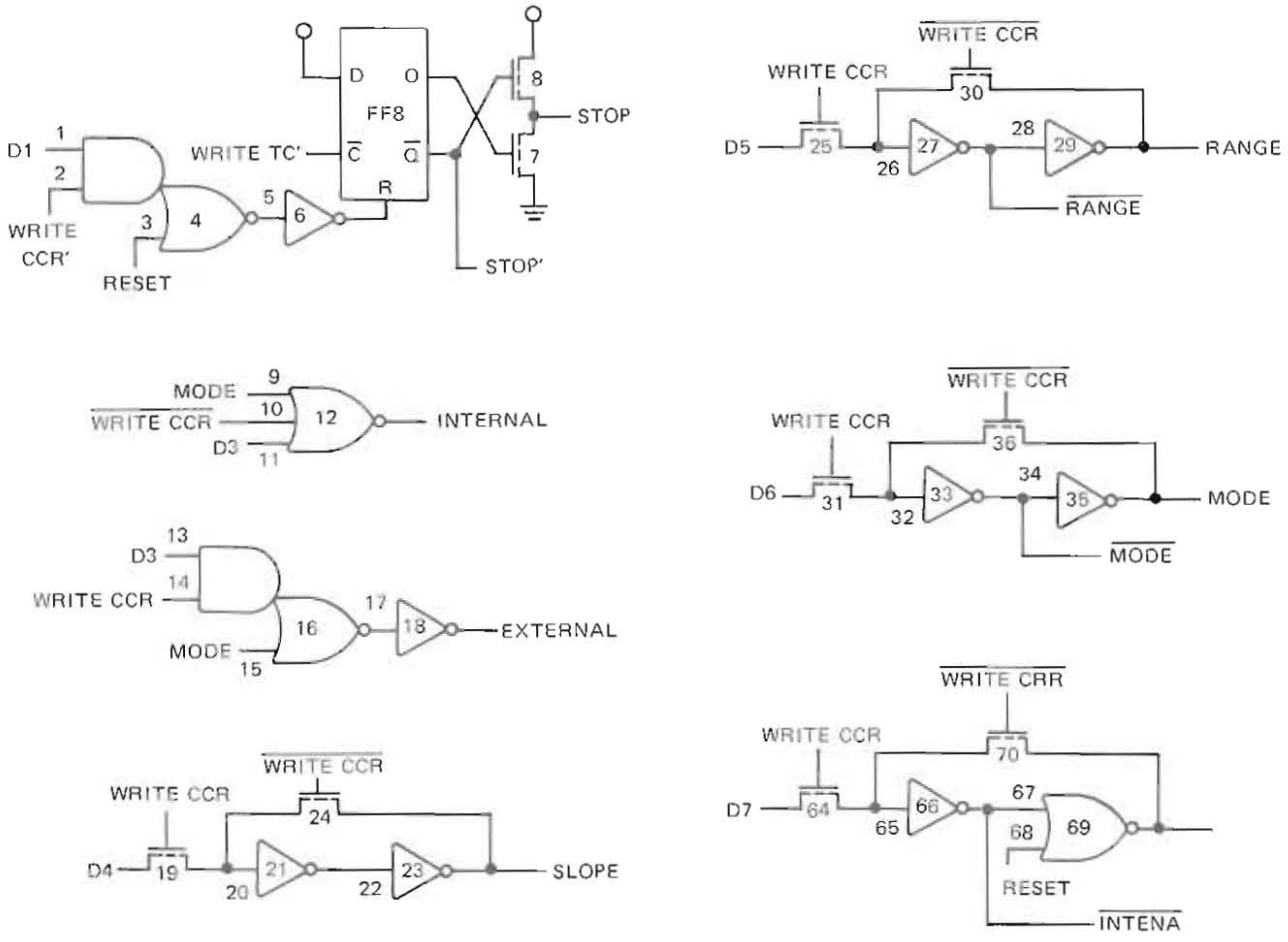
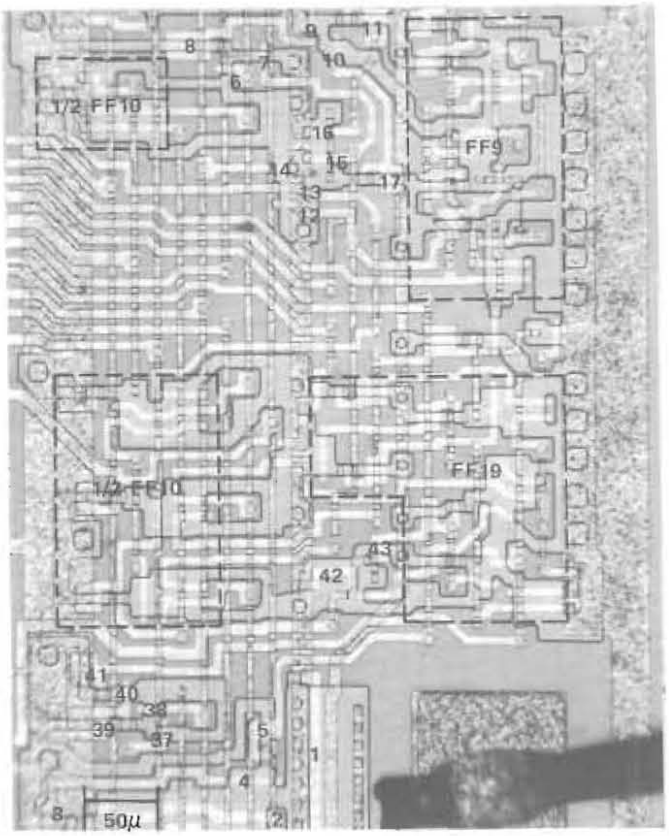


FIGURE 4-10B. ZILOG Z80-CTC CHANNEL CONTROL REGISTER (CHANNEL ϕ).

which discontinues the counter operation. Counting is resumed when a time constant is loaded. Bit 3 controls the timer mode trigger source. If bit 3 = 0, the timer begins operation on the rising edge of Clock. If bit 3 = 1 the external trigger (CLK/TRG) is valid for starting the timer operation following the rising edge of Clock. Note that bits 1 and 3 are not stored conditions.

4.7 - Channel Trigger (CLK/TRG 3 through CLK/TRG 0 Inputs).

The External Clock/Timer Trigger input for channel zero is illustrated in Figure 4-11. The active edge of this input is determined by SLOPE (Bit 4) from the channel control register. In the counter mode, every active edge on this input decrements the down counter. In the timer mode, an active edge initiates the timing function. FF9 latches the trigger input asynchronously, then FF10 synchronizes $\overline{TRG}$ to the rising edge of Clock. The latch formed by transistors 6 through 17 resets FF9. Note that when STOP is "high", FF9 is reset; thus trigger inputs are not recognized when the counter is disabled.



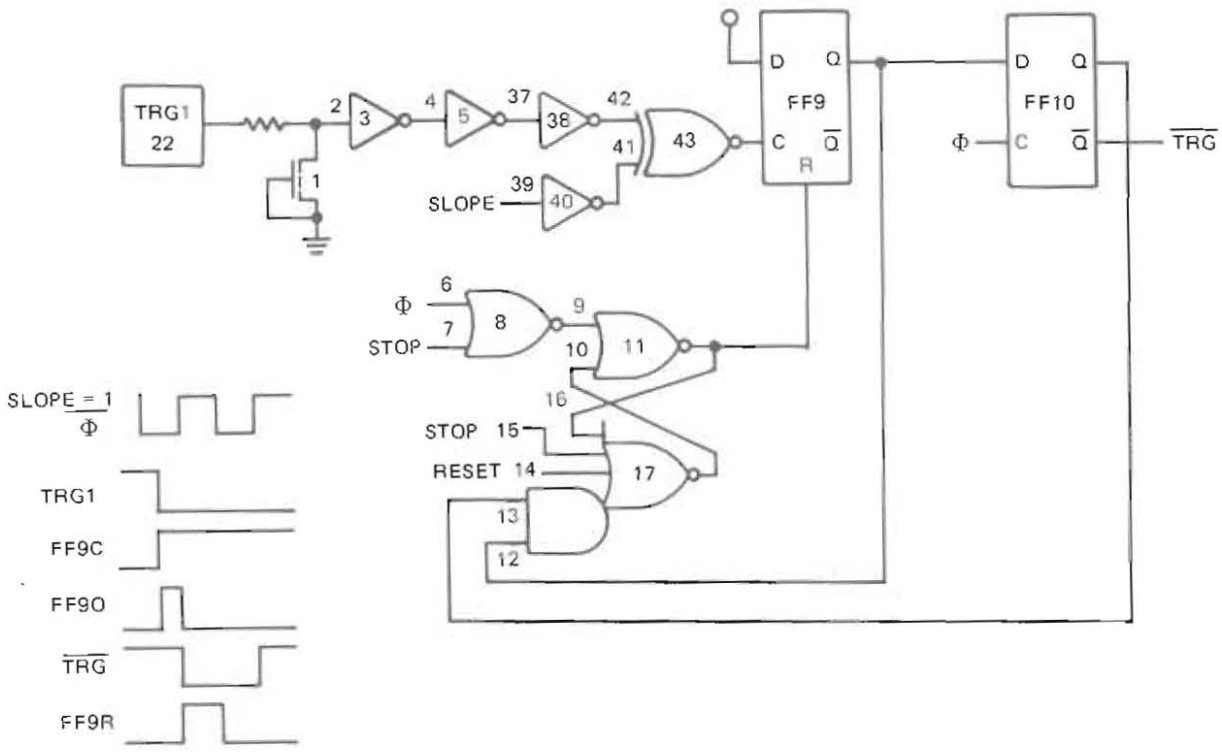
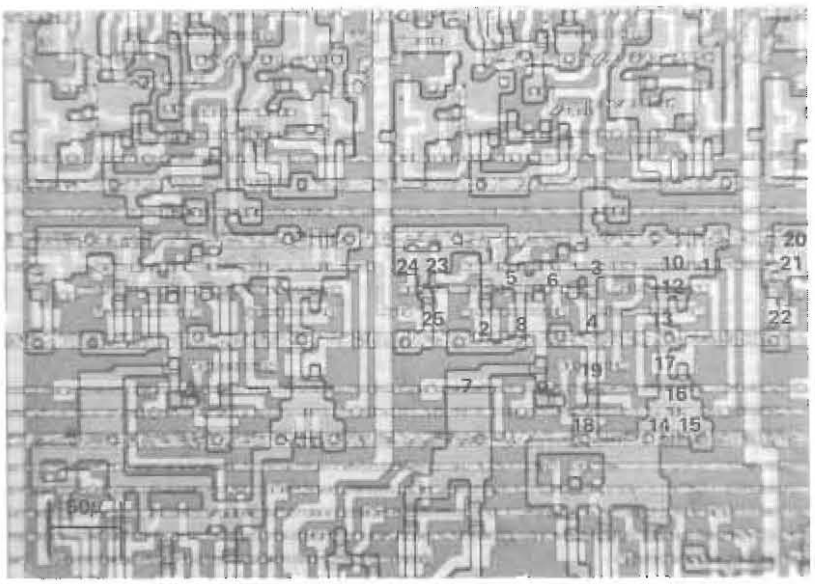


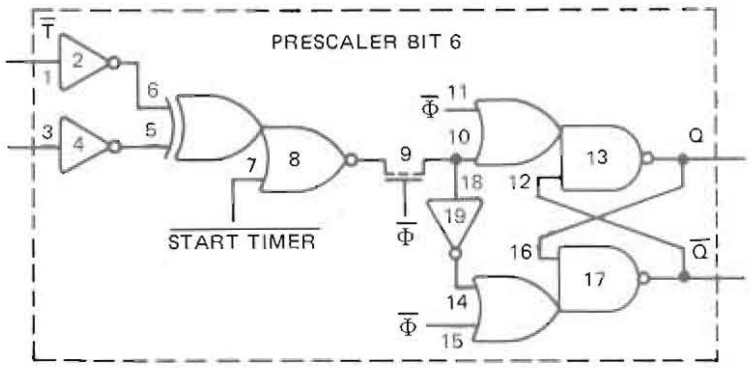
FIGURE 4-11. ZILOG Z80-CTC EXTERNAL CLOCK/TIMER TRIGGER (CLK/TGR ϕ) INPUT.

4.8 - Channel Prescaler, Time Constant Register and Down Counter

In the timer mode, the prescaler is an 8-bit counter which can be programmed by bit 5 of the channel control register to divide the system clock by either 16 or 256. Figure 4-12 illustrates bit 6 of the prescaler. When $\overline{\text{START TIMER}}$ is "high" the prescaler is reset. Transistors 10 through 19 form a latch that changes state on the rising edge of Clock depending on a toggle input (T or $\overline{T}$) and the feedback line from Q or $\overline{Q}$. Figure 4-14 illustrates how the 8 bits of the prescaler are connected. PF16 and PF256 are the prescaler outputs used in the channel counter control described in the next section.

Bit 6 of the time constant register and down counter are illustrated in Figure 4-13. The down counter stage operates in the same manner as the prescaler. WRITE TC loads the time constant register latch formed by transistors 37 through 41. LOAD DC transfers the time constant to the down counter while $\overline{\text{READ DC}}$ transfers the contents of the down counter to the internal data bus. Transistor 55 is part of a zero detect gate. ZERO is an input to the channel interrupt circuitry (Section 4.10). The 8 down counter stages are connected in the same manner as the prescaler (Figure 4-14).





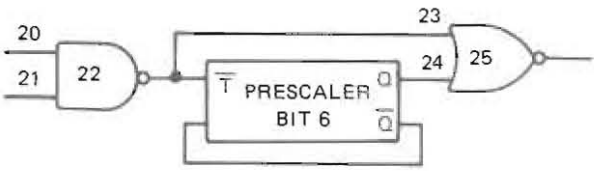
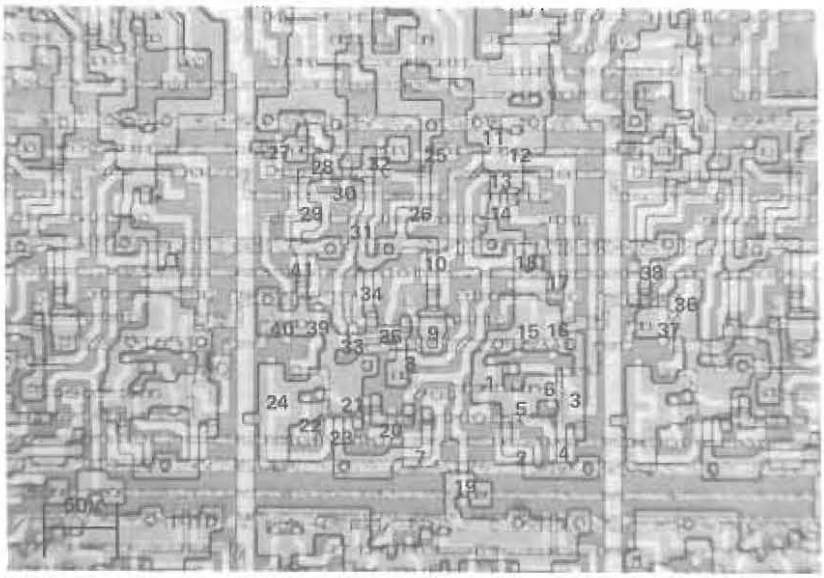
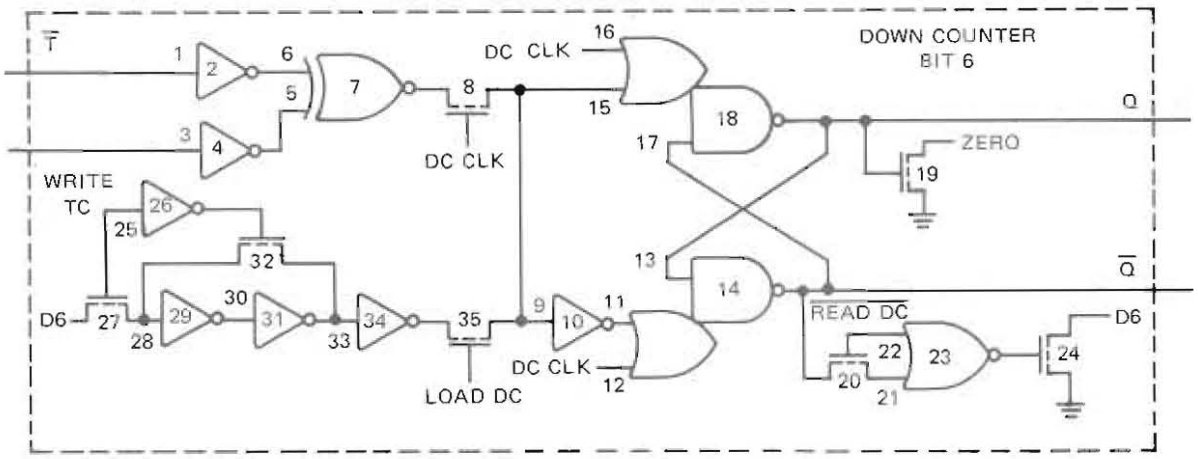


FIGURE 4-12. ZILOG Z80-CTC PRESCALER CELL (BIT 6).





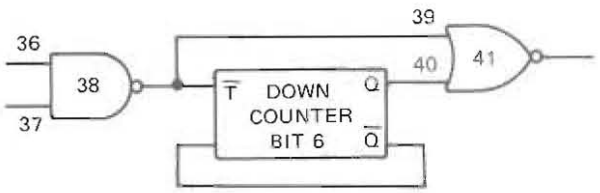


FIGURE 4-13. ZILOG Z80-CTC TIME CONSTANT REGISTER AND DOWN COUNTER CELL (BIT 6).

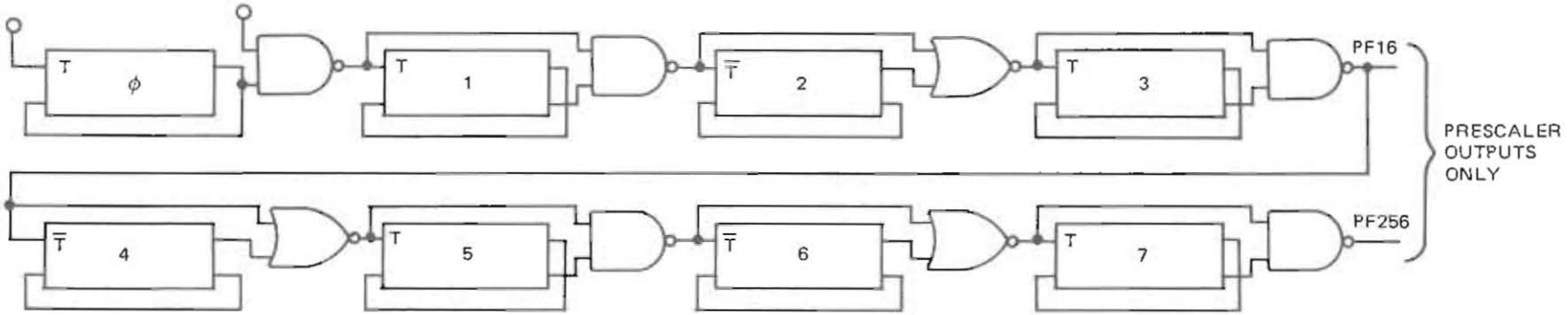


FIGURE 4-14. ZILOG Z80-CTC PRESCALER AND DOWN COUNTER CONFIGURATION.

4.9 - Channel Counter Control

In the counter mode (Bit 6 = 1) the down counter is decremented by each triggering edge of the external Clock input. Figure 4-15 illustrates the circuitry that generates the Clock and Load signals for the prescaler and the down counter. The counter mode is enabled by a NOR gate and an inverter (Transistors 69 through 73). $\overline{TRG}$ becomes the down counter clock (DC CLK) through 2 NOR gates and a non-inverting driver (transistors 74 through 85). In both the counter and the timer mode the down counter is loaded when it reaches a zero count or when the channel stops counting or timing. Transistors 86 through 90 generate the load DC signal whenever STOP or TO1 = 1. (Transistors 80 through 90 are photographed in Figure 4-16).

The timer mode (Bit 6 = 0) is inhibited by a reset condition on FF4 when mode = 1 (See Figure 4-10 channel control register bit 3). When the timer mode is selected the output of the prescaler clocks the down counter. One prescaler output (PF16 or PF256) is selected by the RANGE bit (Transistors 53 through 65). If $\overline{START}$ $\overline{TIMER}$ is enabled by FF14 then the output of FF15 controls DC CLK (transistors 48 through 79 are photographed in Figure 4-10).

An inverting buffer (not photographed) for the system clock drives the prescaler clock.

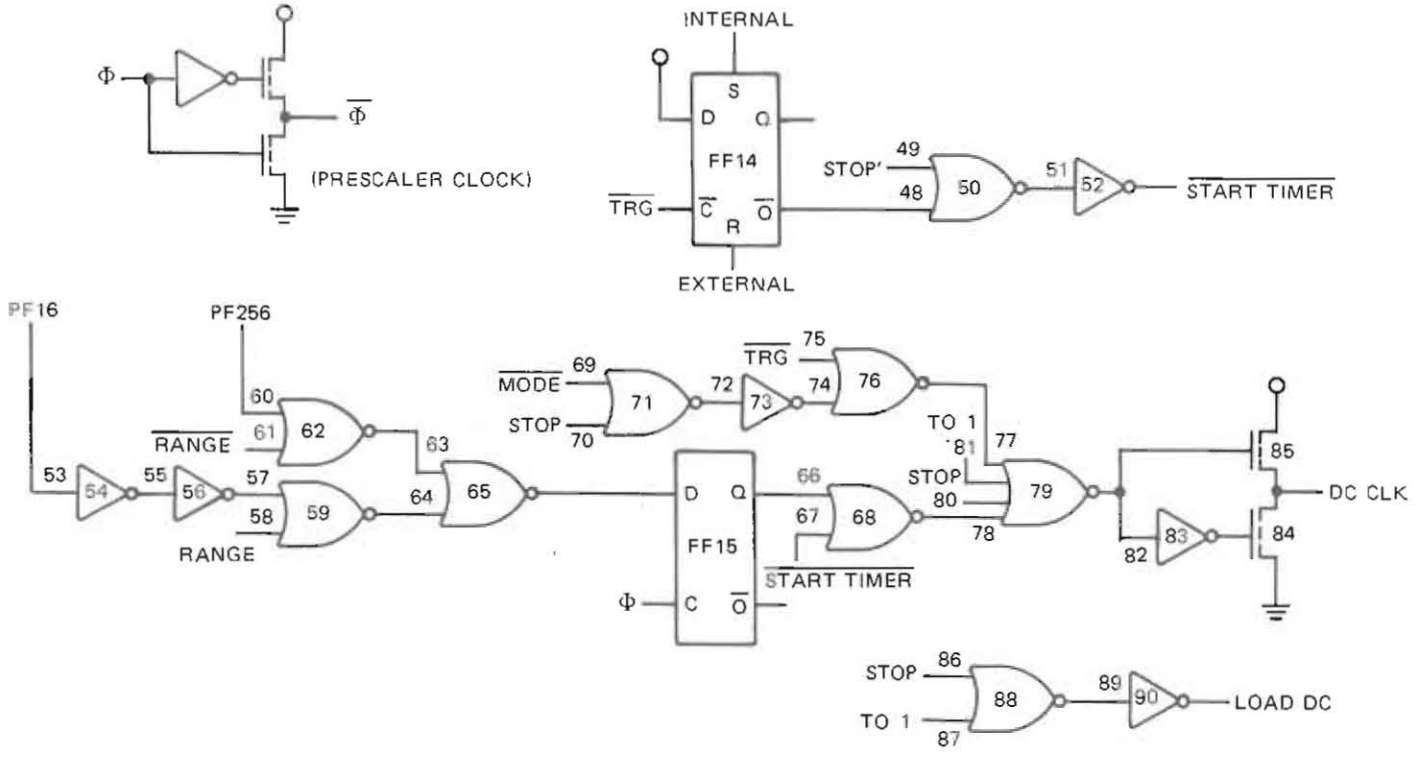


FIGURE 4-15. ZILOG Z80-CTC CHANNEL COUNTER/TIMER CONTROL.

4.10 - Channel Interrupt (ZC/TO_2 through ZC/TO_0 Inputs)

The channel generates a possible interrupt request sequence every time the down counter reaches a zero count condition. Figure 4-16 illustrates the interrupt control circuitry for channel one. FF16 is set when the down counter reaches zero. FF17 delays the zero count signal and resets FF16 when Clock equals "0". Transistors 1 through 12 form a two stage inverting driver for the ZC/TO1 output (Pin 8). The $\overline{Q}$ output of FF17 also is an input to the channel interrupt circuitry that implements the Z80 system of nested priority interrupts. Transistors 19 through 25 latch the zero count condition if the channel interrupt is enabled ($\overline{INTENA}$ = 0) and there is not already an interrupt under service (IUS1 = 0). INT1 goes "high" and generates an Interrupt Request ($\overline{INT}$ = 0) that is "wire-ORed" to the CPU $\overline{INT}$ input.

To ensure that the daisy chain enable lines are stable during an interrupt acknowledge cycle, transistors 31 through 38 latch the interrupt condition only when $\overline{M1}$ is "high". IP1 becomes "high" and is used to inhibit lower priority interrupts as discussed in Section 4.4. ACK1 is used in the Read/Write circuitry to enable reading of the interrupt vector during an interrupt acknowledge cycle. The signal is also an input to the interrupt vector register. The two input NOR gate composed of transistors 55 through 57 is used to reset the interrupt input and set the interrupt-under-service latch (FF18). $\overline{IEI2}$ is

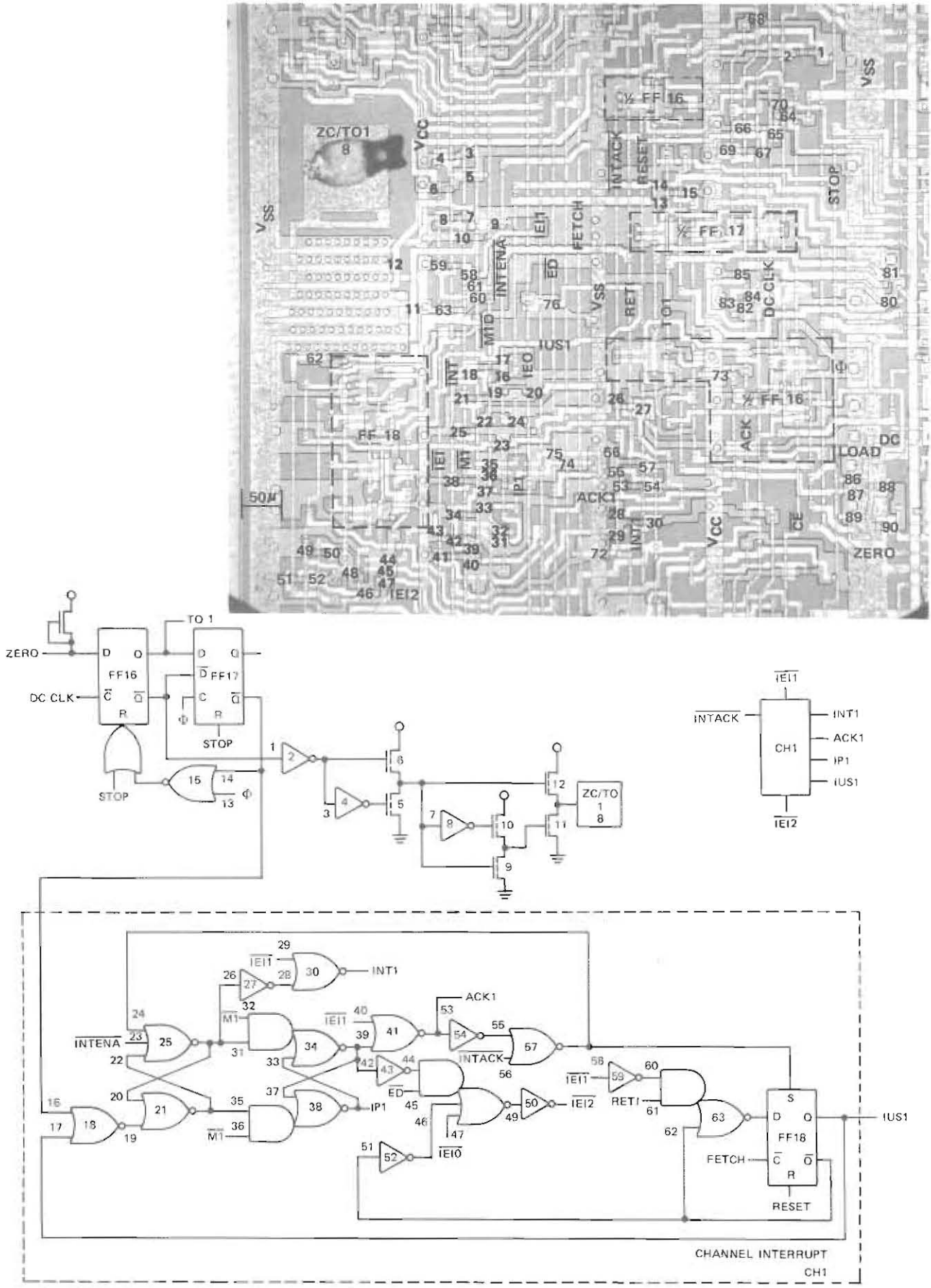


FIGURE 4-16. ZILOG Z80-CTC ZERO COUNT/TIMEOUT (ZC/TO 1) AND CHANNEL INTERRUPT.

generated by transistors 42 through 50 as part of the internal interrupt daisy chain. FF18 is reset at the end of a return from interrupt instruction if there are no higher priority interrupts ($\overline{IEII}$ = 1). Refer to Section 4.4 for a discussion of how the channel interrupt signals are used in CTC interrupt servicing.

SECTION V - SPECIFICATION REVIEW

The information and comments in this section are based on a Zilog Product Specification dated April 1978 included in the Appendix of this report.

The Z80-CTC Features list should include the timer resolution and maximum delay times. These are useful points of comparison among timer circuits. The resolution is 8 microseconds (prescaler ÷ 16) and the maximum delay is 32 milliseconds (prescaler ÷ 256).

The block diagrams in Figures 1 and 2 should separate the internal data bus from the control lines to show more clearly the function of each control line.

Timing Waveforms on pages 3 and 4 show bus timing relationships for each of the CPU cycles. Explanation for the return from interrupt cycle is correct but not clearly written.

The Programming section details the channel operation in both the timer and counter modes. The timer resolution and maximum delay time can be calculated from the formula given under Bit 6 = 0.

A.C. characteristics are shown both for the Z80-CTC (page 6) described in this report and the faster Z80A-CTC (page 7). The maximum clock frequency for the Z80-CTC is 2.5 MHz while the Z80A-CTC is 4MHz. An A.C. Timing Diagram is on page 8.

Absolute Maximum Ratings are listed for the commercial temperature range of 0°C to 70°C. The rating for the voltage on any pin with respect to ground of -0.3V to +7V is specified to insure that the input junctions do not become forward biased (-0.3V) or the input voltage is not greater than the punch-through voltage or field threshold voltages (+7V) which may damage the device. The power dissipation rating of 0.8W is slightly greater than the maximum operating power dissipation [I_{cc} (V_{CC} + 5% V_{CC})] of 0.64W. Power dissipation of 0.8W is adequately conservative for a ceramic package at 70°C ambient.

The DC characteristics include Darlington Drive Current (I_{OHD}) of -1.5 mA at V_{OH} = V_{EXT} = 1.5V. This is the source current available to drive the base of high current transistors in the Darlington configuration.

Capacitance is measured at 1MHz separately for the clock, input pins and output pins. Package capacitance has a significant effect.

SECTION VI - CONCLUSIONS

The Z80-CTC, as well as the Z80 PIO and SIO are not general purpose devices. The control signals are unique to the Z80-CPU, and the additional circuitry required for the interface would not justify using the CTC in other microcomputer systems. Moreover, the CTC relies on the Z80-CPU RETI op codes for interrupt processing.

The maximum timer delay of 32 ms. is a limitation compared to competitive timer circuits.

The daisy chain interrupt structure implemented in the part limits the ability to program the interrupt priority, but has the advantage of reducing software requirements.

The bus timing specifications are critical when designing a system with many peripherals and large memory. Buffers are almost always required to drive the address and data bus. Delay times must be revised and in some cases the system clock speed may have to be reduced.

SECTION VII - RECOMMENDATIONS

If a programmable counter and timer function is needed in a Z80-CPU microprocessor system, the Z80-CTC will be the most favorable choice, since other timer circuits (such as the Intel 8253 Counter/Timer) are not directly compatible with the Z80 control signals.

The time required for testing the Z80-CTC should not be excessive, since the four channels can be tested concurrently. A gate level description of the part is required to estimate the fault coverage of proposed test sequences.

Workmanship exhibited in the samples examined in this report was good. However, traditional military part testing must be continued to catch reoccurring problems such as package lid seal leaks, loose wire bonds and intermetallic formation. Long bonding wires and voids in the die attach area are potential reliability hazards encountered in this examination (Section II).

Chip temperatures and metal current densities should be re-evaluated for any versions of this part specified for higher temperature ambients.

Z80®-CTC
Z80®A-CTC

Zilog

Product Specification

APRIL 1978

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The Z80-Counter Timer Circuit (CTC) is a programmable, four channel device that provides counting and timing functions for the Z80-CPU. The Z80-CPU configures the Z80-CTC's four independent channels to operate under various modes and conditions as required.

Structure

- N-Channel Silicon Gate Depletion Load Technology
- 28 Pin DIP
- Single 5 volt supply
- Single phase 5 volt clock
- Four independent programmable 8-bit counter/16-bit timer channels

Features

- Each channel may be selected to operate in either a counter mode or timer mode.
- Programmable interrupts on counter or timer states.
- A time constant register automatically reloads the down counter at zero and the cycle is repeated.
- Readable down counter indicates number of counts-to-go until zero.
- Selectable 16 or 256 clock prescaler for each timer channel.
- Selectable positive or negative trigger may initiate timer operation.
- Three channels have zero count/timeout ontputs capable of driving Darlington transistors.
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic.
- All inputs and outputs fully TTL compatible.
- Outputs directly compatible with Z80-SIO.

CTC Architecture

A block diagram of the Z80-CTC is shown in figure 1. The internal structure of the Z80-CTC consists of a Z80-CPU bus interface, internal control logic, four counter channels, and interrupt control logic. Each channel has an interrupt vector for automatic interrupt vectoring, and interrupt priority is determined by channel number with channel Ø having the highest priority.

The channel logic is composed of 2 registers, 2 counters and control logic as shown in figure 2. The registers include an 8-bit time constant register and an 8-bit channel control register. The counters include an 8-bit readable down counter and an 8-bit prescaler. The prescaler may be programmed to divide the system clock by either 16 or 256.

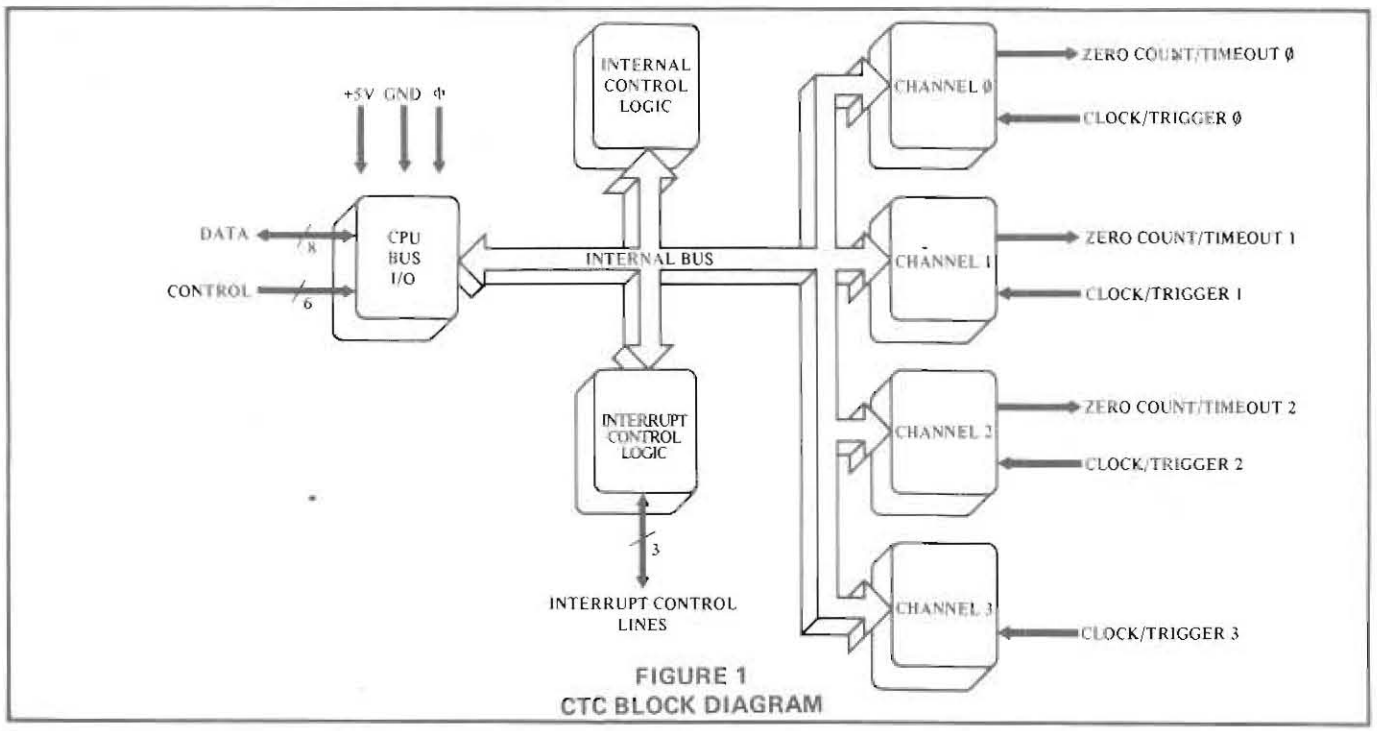


FIGURE 1
CTC BLOCK DIAGRAM

Channel Counter and Register Description

Time Constant Register – 8 bits, loaded by the CPU to initialize and re-load Down Counter at a count of zero.

Channel Control Register – 8 bits, loaded by the CPU to select the mode and conditions of channel operation.

Down Counter – 8 bits, loaded by the Time Constant Register under program control and automatically at a count of zero. At any time, the CPU can read the number of counts-to-go until a zero count. This counter is decremented by the prescaler in timer mode and CLK/TRIG in counter mode.

Prescaler – 8 bit counter, divides system clock by 16 or 256 for decrementing Down Counter. It is used in timer mode only.

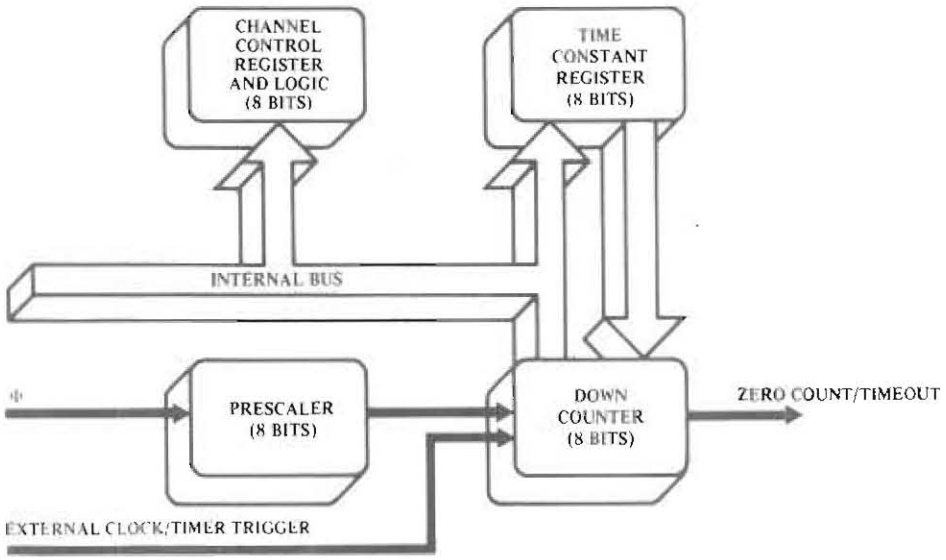
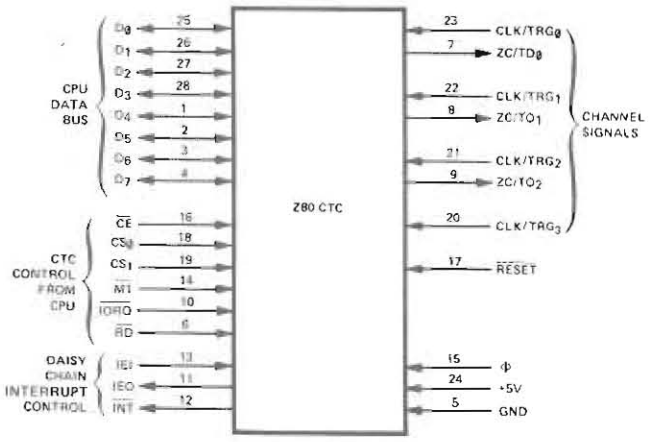


FIGURE 2
CHANNEL BLOCK DIAGRAM

Z80-CTC Pin Description



$CLK/TRG_{\emptyset}$	Channel Ø External Clock or Timer Trigger (Input)
CLK/TRG_1	Channel 1 External Clock or Timer Trigger (Input)
CLK/TRG_2	Channel 2 External Clock or Timer Trigger (Input)
CLK/TRG_3	Channel 3 External Clock or Timer Trigger (Input)
$ZC/TO_{\emptyset}$	Channel Ø Zero Count or Timeout (output, active high)

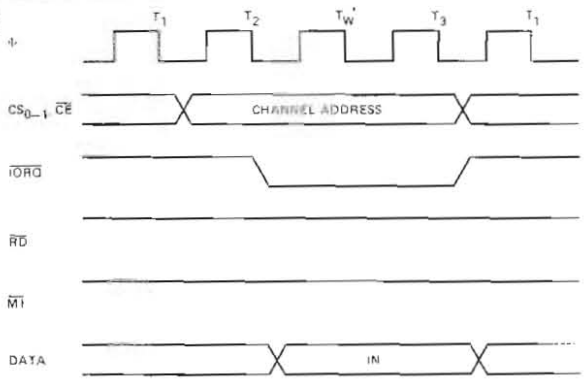
Z80-CTC Pin Description (continued)

ZC/TO_1	Channel 1 Zero Count or Timeout (output, active high)
ZC/TO_2	Channel 2 Zero Count or Timeout (output, active high)
$CS_1 - CS_\emptyset$	Channel Select (input, active high). These form a 2-bit binary address of the channel to be accessed.
$D7 - D_\emptyset$	Z80-CPU Data Bus (bidirectional, tristate)
$\overline{CE}$	Chip Enable (input, active low)
Φ	System Clock (input)
$\overline{M1}$	Machine Cycle One Signal from Z80-CPU (input, active low)
$\overline{IORQ}$	Input/Output Request from Z80-CPU (input, active low)
$\overline{RD}$	Read Cycle Status from the Z80-CPU (input, active low)
IEI	Interrupt Enable In (input, active high)
IEO	Interrupt Enable Out (output, active high). IEI and IEO form a daisy chain connection for priority interrupt control
$\overline{INT}$	Interrupt Request (output, open drain, active low)
$\overline{RESET}$	RESET stops all channels from counting and resets channel interrupt enable bits in all control registers. During reset time $ZC/TO_{\emptyset-2}$ and $\overline{INT}$ go to the inactive states, IEO reflects the state of IEI, and the data bus output drivers go to the high impedance state (input, active low)

Timing Waveforms

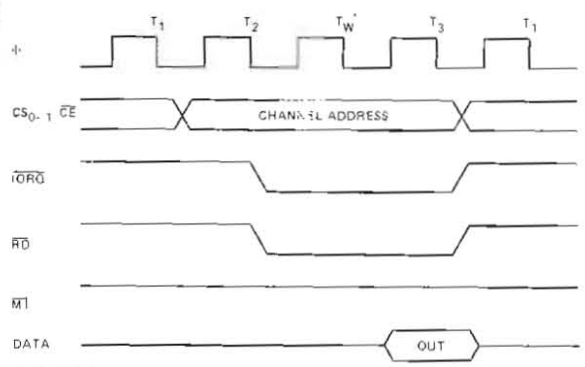
CTC WRITE CYCLE

Illustrated here is the timing for loading a channel control word, time constant and interrupt vector. No wait states are allowed for writing to the CTC other than the automatically inserted (T_W*). Since the CTC does not receive a specific write signal, it internally generates its own from the lack of an $\overline{RD}$ signal.



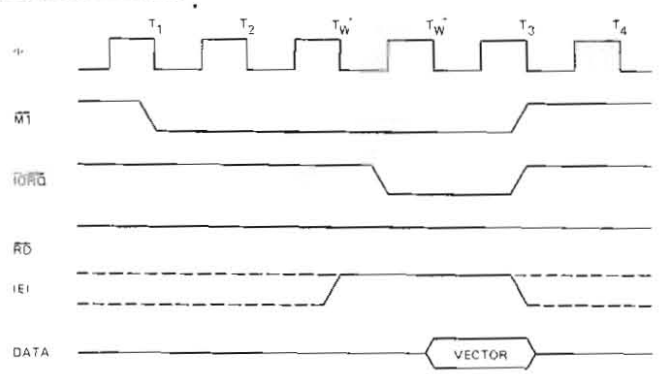
CTC READ CYCLE

Illustrated here is the timing for reading a channel's Down Counter when in Counter Mode. The value read onto the data bus reflects the number of external clock's rising edges prior to the rising edge of cycle (T_2). No wait states are allowed for reading the CTC other than the automatically inserted (T_W*).



INTERRUPT ACKNOWLEDGE CYCLE

Some time after an interrupt is requested by the CTC, the CPU will send out an interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$). During this time the interrupt logic of the CTC will determine the highest priority channel which is requesting an interrupt. To insure that the daisy chain enable lines stabilize, channels are inhibited from changing their interrupt request status when $\overline{M1}$ is active. If the CTC Interrupt Enable Input (IEI) is active, then the highest priority interrupting channel places the contents of its interrupt vector register onto the Data Bus when $\overline{IORQ}$ goes active. Additional wait cycles are allowed.



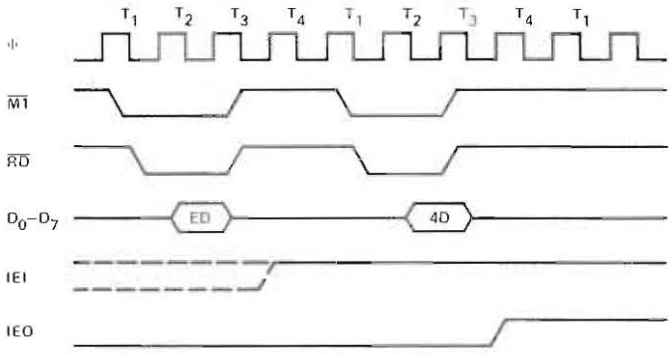
Timing Waveforms (continued)

RETURN FROM INTERRUPT CYCLE

If a Z80 peripheral device has no interrupt pending and is not under service, then its IEO = IEI. If it has an interrupt under service (i.e. it has already interrupted and received an interrupt acknowledge) then its IEO is always low, inhibiting lower priority chips from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO will be low unless an "ED" is decoded as the first byte of a two byte opcode. In this case, IEO will go high until the next opcode byte is decoded, whereupon it will again go low. If the second byte of the opcode was a "4D" then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service will have its IEI high and its IEO low. This device is the highest priority device in the daisy chain which has received an interrupt acknowledge. All other peripherals have IEI = IEO. If the next opcode byte decoded is "4D", this peripheral device will reset its "interrupt under service" conditiou.

Wait cycles are allowed in the $\overline{M1}$ cycles.



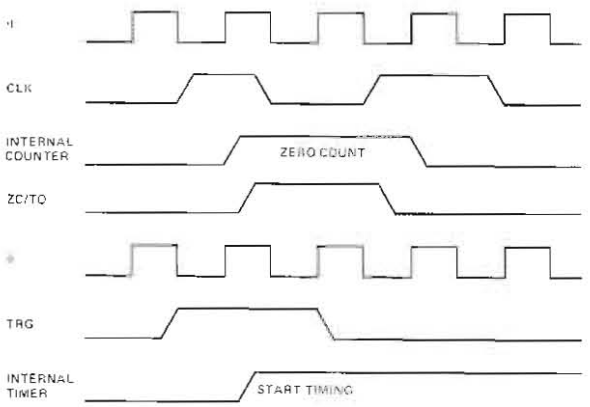
DAISY CHAIN INTERRUPT SERVICING

Illustrated at right is a typical nested interrupt sequence which may occur in the CTC. In this sequence channel 2 interrupts and is granted service. While this channel is being serviced, higher priority channel 1 interrupts and is granted service. The service routine for the higher priority channel is completed and a RETI instruction is executed to indicate to the channel that its routine is complete. At this time the service routine of lower priority channel 2 is completed.

CTC COUNTING AND TIMING

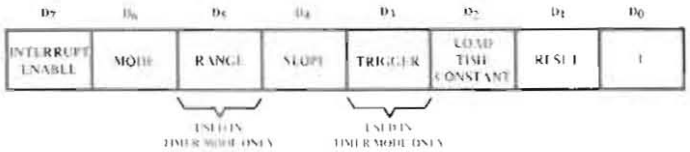
In the counter mode the rising or falling edge of the CLK input causes the counter to be decremented. The edge is detected totally asynchronously and must have a minimum CLK pulse width. However, the counter is synchronous with Φ therefore a setup time must be met when it is desired to have the counter decremented by the next rising edge of Φ.

In the timer mode the prescaler may be enabled by a rising or falling edge on the TRG input. As in the counter mode, the edge is detected totally asynchronously and must have a minimum TRG pulse width. However, when timing is to start with respect to the next rising edge of Φ a setup time must be met. The prescaler counts rising edges of Φ.



SELECTING AN OPERATING MODE

When selecting a channel's operating mode, bit Ø is set to 1 to indicate this word is to be stored in the channel control register.



Bit 7 = Ø — Channel interrupts disabled.

Bit 7 = 1 — Channel interrupts enabled to occur every time Down Counter reaches a count of zero. Setting Bit 7 does not let a preceding count of zero cause an interrupt.

Bit 6 = Ø — Timer Mode – Down counter is clocked by the prescaler. The period of the counter is:
$t_C \bullet P \bullet TC$
t_C = system clock period
P = prescale of 16 or 256
TC = 8 bit binary programmable time constant (256 max)

Bit 6 = 1 — Counter Mode – Down Counter is clocked by external clock. The prescaler is not used.

Bit 5 = Ø — Timer Mode Only–System clock Φ is divided by 16 in prescaler.

Bit 5 = 1 — Timer Mode Only–System clock Φ is divided by 256 in prescaler.

Bit 4 = Ø — Timer Mode – negative edge trigger starts timer operation.
Counter Mode – negative edge decrements the down counter.

Bit 4 = 1 — Timer Mode – positive edge trigger starts timer operation.
Counter Mode – positive edge decrements the down counter.

Bit 3 = Ø — Timer Mode Only – Timer begins operation on the rising edge of T_2 of the machine cycle following the one that loads the time constant.

Bit 3 = 1 — Timer Mode Only – External trigger is valid for starting timer operation after rising edge of T_2 of the machine cycle following the one that loads the time constant. The Prescaler is decremented 2 clock cycles later if the setup time is met, otherwise 3 clock cycles.

Bit 2 = Ø — No time constant will follow the channel control word. One time constant must be written to the channel to initiate operation.

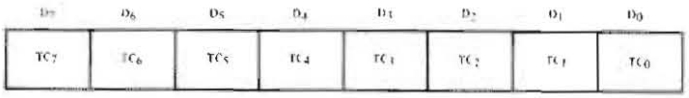
Bit 2 = 1 — The time constant for the Down Counter will be the next word written to the selected channel. If a time constant is loaded while a channel is counting, the present count will be completed before the new time constant is loaded into the Down Counter.

Bit 1 = Ø — Channel continues counting.

Bit 1 = 1 — Stop operation. If Bit 2 = 1 channel will resume operation after loading a time constant, otherwise a new control word must be loaded.

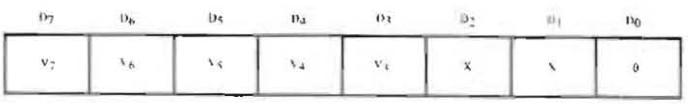
LOADING A TIME CONSTANT

An 8-bit time constant is loaded into the Time Constant register following a channel control word with bit 2 set. All zeros indicate a time constant of 256.



LOADING AN INTERRUPT VECTOR

The Z80-CPU requires that an 8-bit interrupt vector be supplied by the interrupting channel. The CPU forms the address for the interrupt service routine of the channel using this vector. During an interrupt acknowledge cycle the vector is placed on the Z80 Data Bus by the highest priority channel requesting service at that time. The desired interrupt vector is loaded into the CTC by writing into channel Ø with a zero in DØ. D7-D3 contain the stored interrupt vector, D_2 and D_1 are not used in loading the vector. When the CTC responds to an interrupt acknowledge, these two bits contain the binary code of the highest priority channel which requested the interrupt and DØ contains a zero since the address of the interrupt service routine starts at an even byte. Channel Ø is the highest priority channel.

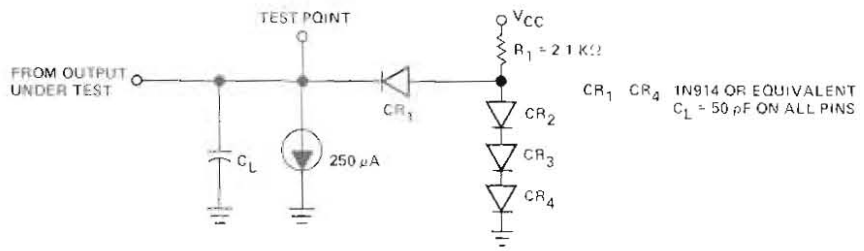


TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

Signal	Symbol	Parameter	Min	Max	Unit	Comments
Φ	t_C	Clock Period	400	[1]	ns	
	$t_W(\Phi H)$	Clock Pulse Width, Clock High	170	2000	ns	
	$t_W(\Phi L)$	Clock Pulse Width, Clock Low	170	2000	ns	
	t_r, t_f	Clock Rise and Fall Times		30	ns	
	t_H	Any Hold Time for Specified Setup Time	0		ns	
CS, $\overline{CE}$, etc	$t_{S\Phi}(CS)$	Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle	160		ns	
D_0–D_7	$t_{DR}(D)$	Data Output Delay from Rising Edge of $\overline{RD}$ During Read Cycle		480	ns	[2]
	$t_{S\Phi}(D)$	Data Setup Time to Rising Edge of Φ During Write or M1 Cycle	60		ns	
	$t_{DI}(D)$	Data Output Delay from Falling Edge of IORO During INTA Cycle		340	ns	[2]
	$t_F(D)$	Delay to Floating Bus (Output Buffer Disable Time)		230	ns	
IEI	$t_S(IEI)$	IEI Setup Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	200		ns	
IEO	$t_{DH}(IO)$	IEO Delay Time from Rising Edge of IEI		220	ns	[3]
	$t_{DL}(IO)$	IEO Delay Time from Falling Edge of IEI		190	ns	[3]
	$t_{DM}(IO)$	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring just Prior to $\overline{M1}$)		300	ns	[3]
$\overline{IORQ}$	$t_{S\Phi}(IR)$	$\overline{IORQ}$ Setup Time to Rising Edge of Φ During Read or Write Cycle	250		ns	
$\overline{M1}$	$t_{S\Phi}(M1)$	$\overline{M1}$ Setup Time to Rising Edge of Φ During INTA or M1 Cycle	210		ns	
$\overline{RD}$	$t_{S\Phi}(RD)$	$\overline{RD}$ Setup Time to Rising Edge of Φ During Read or M1 Cycle	240		ns	
$\overline{INT}$	$t_{DCK}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of CLK/TRG		$2t_C(\Phi) + 200$		Counter Mode
	$t_{D\Phi}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of Φ		$t_C(\Phi) + 200$		Timer Mode
CLK/TRG_{0-3}	$t_C(CK)$	Clock Period	$2t_C(\Phi)$			Counter Mode
	t_r, t_f	Clock and Trigger Rise and Fall Times		50		
	$t_S(CK)$	Clock Setup Time to Rising Edge of Φ for Immediate Count	210			Counter Mode
	$t_S(TR)$	Trigger Setup Time to Rising Edge of Φ for Enabling of Prescaler on Following Rising Edge of Φ	210			Timer Mode
	$t_W(CTH)$	Clock and Trigger High Pulse Width	200			Counter and Timer Modes
	$t_W(CTL)$	Clock and Trigger Low Pulse Width	200			Counter and Timer Modes
ZC/TO_{0-2}	$t_{DH}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High		190		Counter and Timer Modes
	$t_{DL}(ZC)$	ZC/TO Delay Time from Falling Edge of Φ, ZC/TO Low		190		Counter and Timer Modes

Notes: [1] $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$.
[2] Increase delay by 10 nsec for each 50 pF increase in loading, 200 pF maximum for data lines and 100 pF for control lines.
[3] Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum
[4] $\overline{RESET}$ must be active for a minimum of 3 clock cycles.

OUTPUT LOAD CIRCUIT

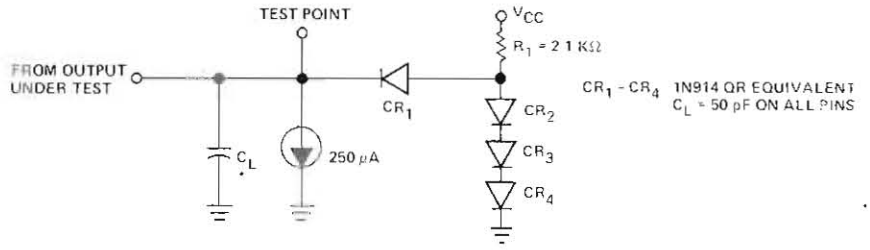


$T_A = 0°$ C to $70°$ C, $V_{CC} = +5$ V ± 5%, unless otherwise noted

Signal	Symbol	Parameter	Min	Max	Unit	Comments
Φ	t_C	Clock Period	250	[1]	ns	
	$t_W(\Phi H)$	Clock Pulse Width, Clock High	105	2000	ns	
	$t_W(\Phi L)$	Clock Pulse Width, Clock Low	105	2000	ns	
	t_r, t_f	Clock Rise and Fall Times		30	ns	
	t_H	Any Hold Time for Specified Setup Time	0		ns	
CS, $\overline{CE}$, etc	$t_{S\Phi}(CS)$	Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle	60		ns	
D_0–D_7	$t_{DR}(D)$	Data Output Delay from Falling Edge of $\overline{RD}$ During Read Cycle		380	ns	[2]
	$t_{S\Phi}(D)$	Data Setup Time to Rising Edge of Φ During Write or M1 Cycle	50		ns	
	$t_{DI}(D)$	Data Output Delay from Falling Edge of IORG During INTA Cycle		160	ns	[2]
	$t_F(D)$	Delay to Floating Bus (Output Buffer Disable Time)		110	ns	
IEI	$t_S(IEI)$	IEI Setup Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	140		ns	
IEO	$t_{DH}(IO)$	IEO Delay Time from Rising Edge of IEI		160	ns	[3]
	$t_{DL}(IQ)$	IEO Delay Time from Falling Edge of IEI		130	ns	[3]
	$t_{DM}(IO)$	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring just Prior to $\overline{M1}$)		190	ns	[3]
$\overline{IORQ}$	$t_{S\Phi}(IR)$	$\overline{IORQ}$ Setup Time to Rising Edge of Φ During Read or Write Cycle	115		ns	
$\overline{M1}$	$t_{S\Phi}(M1)$	$\overline{M1}$ Setup Time to Rising Edge of Φ During INTA or M1 Cycle	90		ns	
$\overline{RD}$	$t_{S\Phi}(RD)$	$\overline{RD}$ Setup Time to Rising Edge of Φ During Reed or M1 Cycle	115		ns	
$\overline{INT}$	$t_{DCK}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of CLK/TRG		$2t_C(\Phi) + 140$		Counter Mode
	$t_{D\Phi}(IT)$	$\overline{INT}$ Delay Time from Rising Edge of Φ		$t_C(\Phi) + 140$		Timer Mode
CLK/TRG_{0-3}	$t_C(CK)$	Clock Period	$2t_C(\Phi)$			Counter Mode
	t_r, t_f	Clock and Trigger Rise and Fall Times		50		
	$t_S(CK)$	Clock Setup Time to Rising Edge of Φ for Immediate Count	210			Counter Mode
	$t_S(TR)$	Trigger Setup Time to Rising Edge of Φ for enabling of Prescaler on Following Rising Edge of Φ	210			Timer Mode
	$t_W(CTH)$	Clock and Trigger High Pulse Width	200			Counter and Timer Modes
	$t_W(CTL)$	Clock and Trigger Low Pulse Width	200			Counter and Timer Modes
ZC/TO_{0-2}	$t_{DH}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High		190		Counter and Timer Modes
	$t_{DL}(ZC)$	ZC/TO Delay Time from Falling Edge of Φ, ZC/TO Low		190		Counter and Timer Modes

Notes: [1] $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$.
[2] Increase delay by 10 nsec for each 50 pF increase in loading, 200 pF maximum for data lines and 100 pF for control lines.
[3] Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum
[4] $\overline{RESET}$ must be active for a minimum of 3 clock cycles.

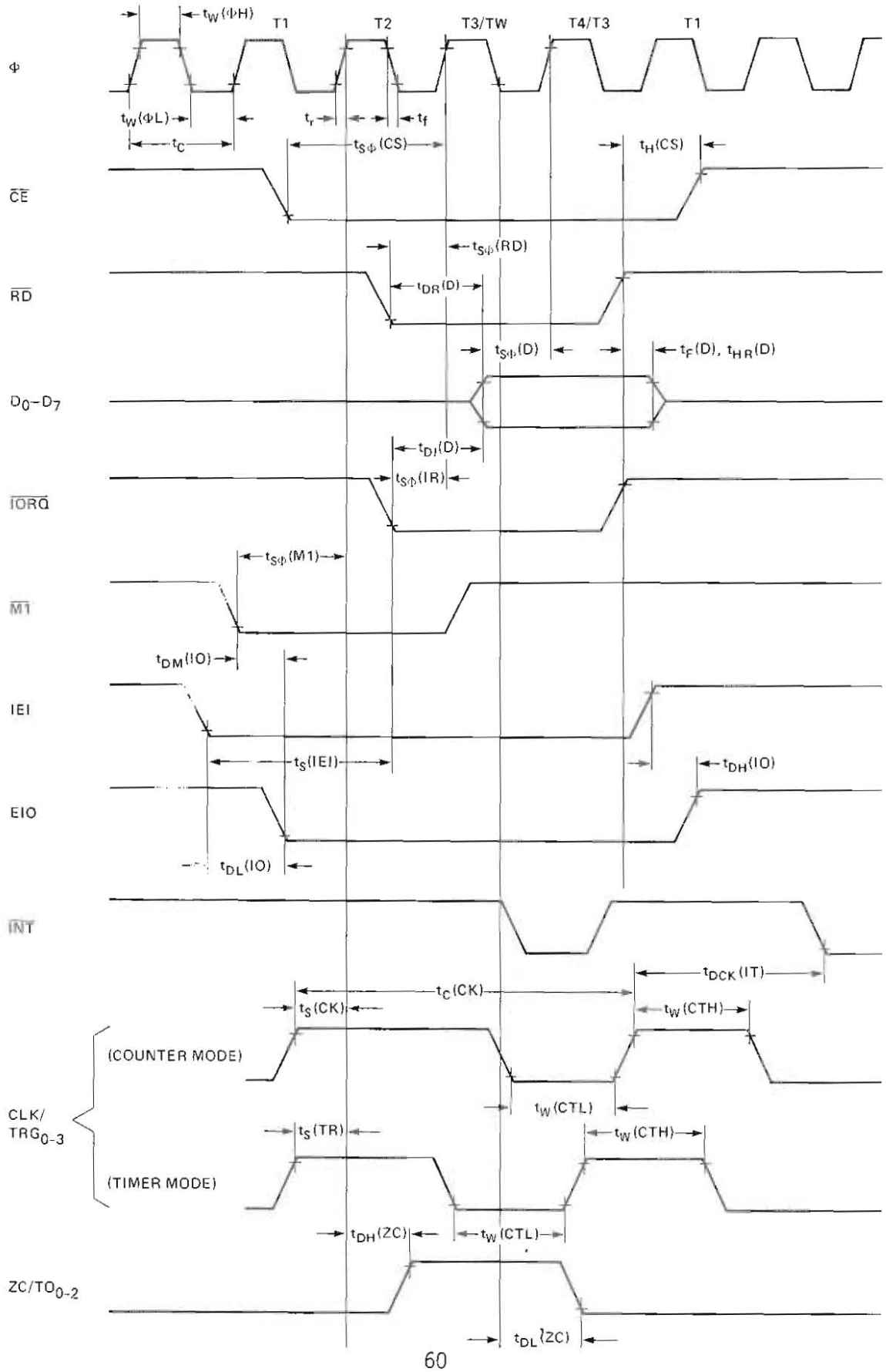
OUTPUT LOAD CIRCUIT



A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{CC} - .6V	.45V
OUTPUT	2.0V	.8V
INPUT	2.0V	.8V
FLOAT	ΔV	±0.5V



Absolute Maximum Ratings

Temperature Under Bias	0° C to 70° C
Storage Temperature	−65° C to +150° C
Voltage On Any Pin With Respect To Ground	−0.3 V to +7 V
Power Dissipation	0.8W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0° C to 70° C, V_{CC} = 5 V ± 5% unless otherwise specified

Z80-CTC

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3	.45	V	
V_{IHC}	Clock Input High Voltage [1]	V_{CC} − .6	V_{CC} + .3	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −250 μA
I_{CC}	Power Supply Current		120	mA	T_C = 400 nsec
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		−10	μA	V_{OUT} = 0.4V
I_{OHD}	Darlington Drive Current	−1.5		mA	V_{EXT} = 1.5V R_{EXT} = 390Ω

Z80A-CTC

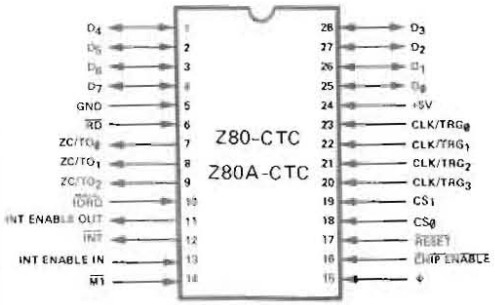
Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3	.45	V	
V_{IHC}	Clock Input High Voltage [1]	V_{CC} − .6	V_{CC} + .3	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −250 μA
I_{CC}	Power Supply Current		120	mA	T_C = 250 nsec
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		−10	μA	V_{OUT} = 0.4V
I_{OHD}	Darlington Drive Current	−1.5		mA	V_{EXT} = 1.5V R_{EXT} = 390Ω

Capacitance

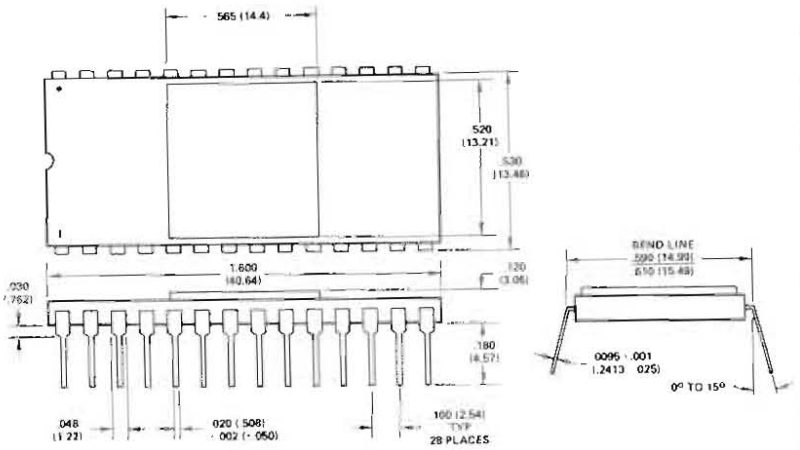
T_A = 25° C, f = 1 MHz

Symbol	Parameter	Max.	Unit	Test Condition
C_Φ	Clock Capacitance	20	pF	Unmeasured Pins Returned to Ground
C_{IN}	Input Capacitance	5	pF	
C_{OUT}	Output Capacitance	10	pF	

Package Configuration



Package Outline



* DIMENSIONS FOR METRIC SYSTEM IN PARENTHESES (mm)

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03-0031-02

Printed in U.S.A.